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MS-7733 Mini ITX Ver: 1.0

Intel -MahoBay plamform

CPU:

INTEL-Ivy bridge LGA1155

System Chipset:

INTEL-Panther Point

OnBoard Chipset:

HD Audio Codec:RTL892

LAN-Lewisville 82579

SIO:Fintek F171808A

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

SO-DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X4) Slot * 1

PWM:

VRD12 - ISL6364CR+1Phase

ACPI:

UPI

Other:

SATA(SATA2-300MB/s) *4

ESATA *2

USB2.0 *6

REAL USB3.0 *2

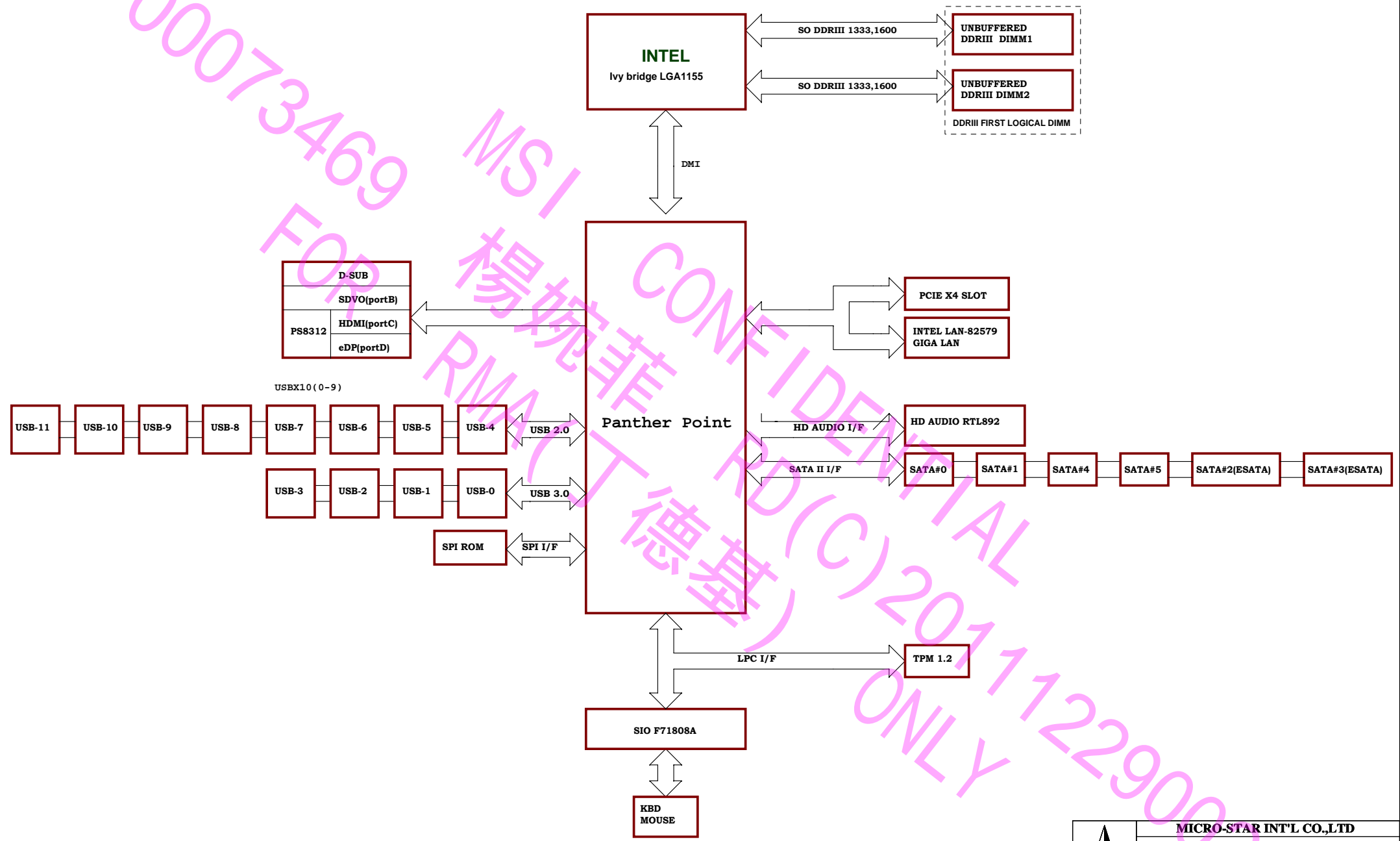
FRONT USB3.0 *2

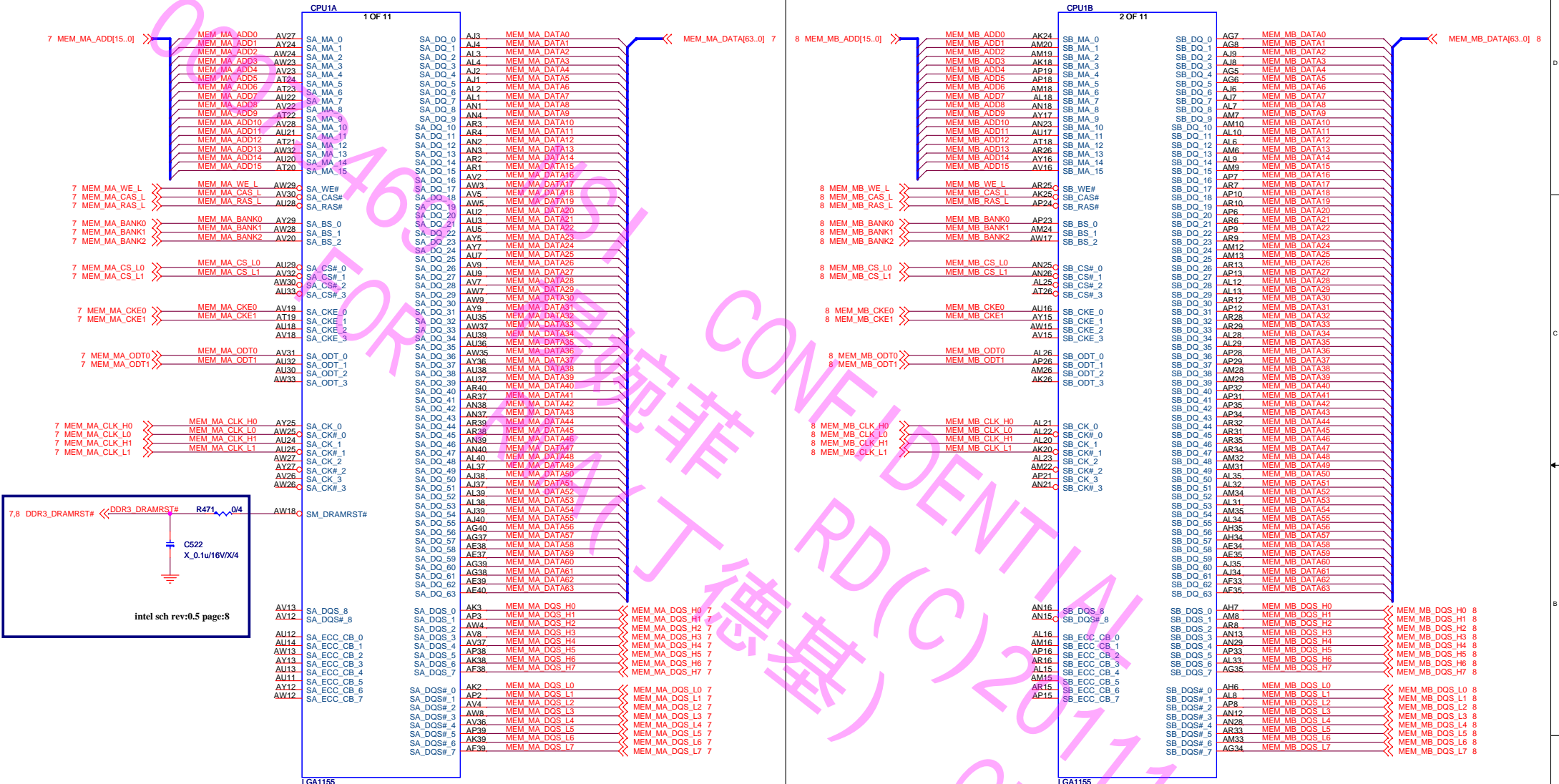


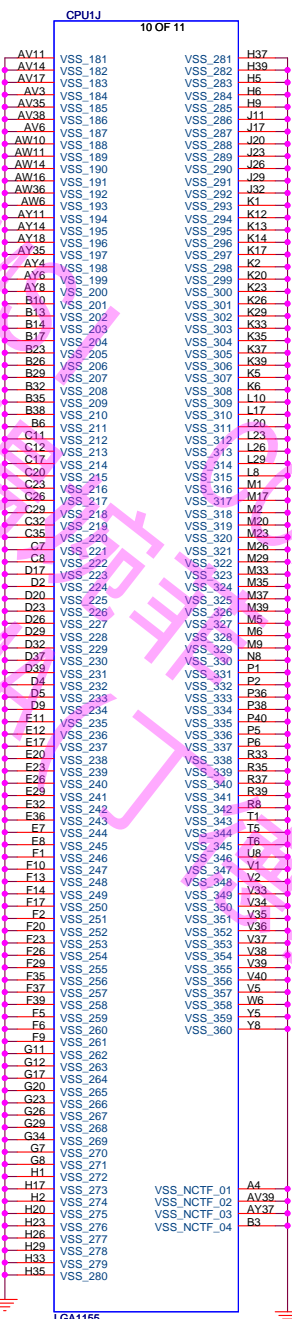
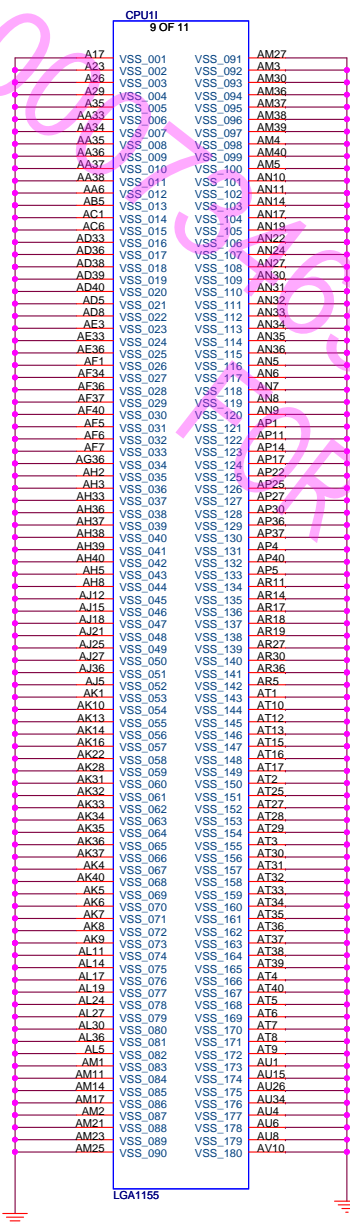
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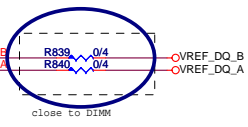
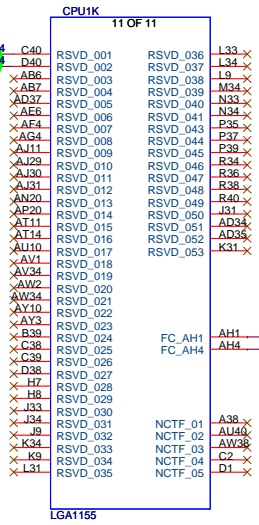






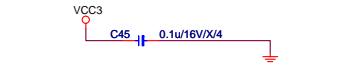
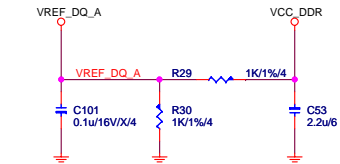
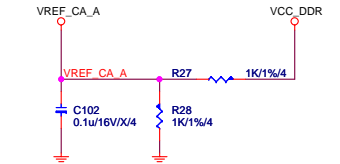
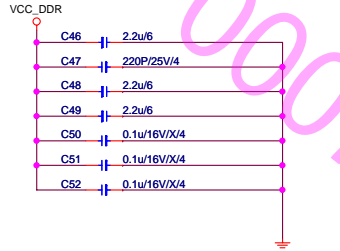
9.34 XDP_CPU_BCLK_P XDP_CPU_BCLK_P
9.34 XDP_CPU_BCLK_N XDP_CPU_BCLK_N

CRB 0.7 107 page

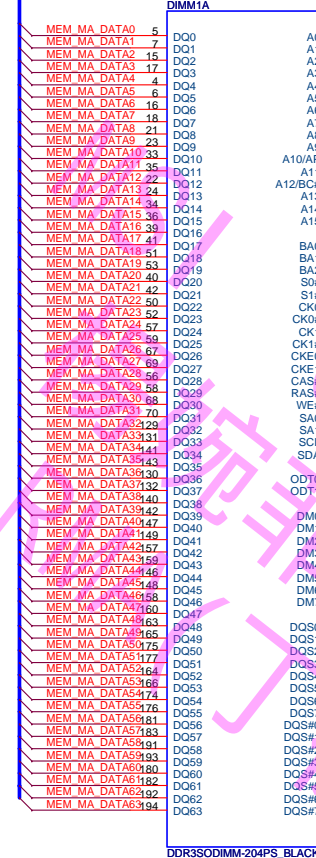


SO_DDRIII DIMM_A0

Place close to DIMM1



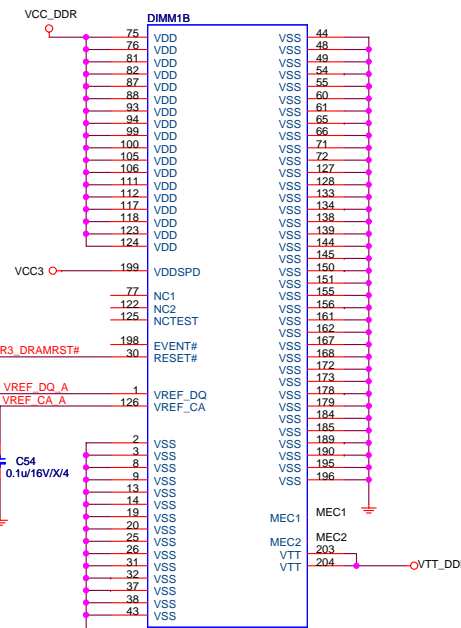
4 MEM_MA_DATA[63..0] <<> MEM_MA_DATA[63..0]



DDR3SODIMM-204PS_BLACK

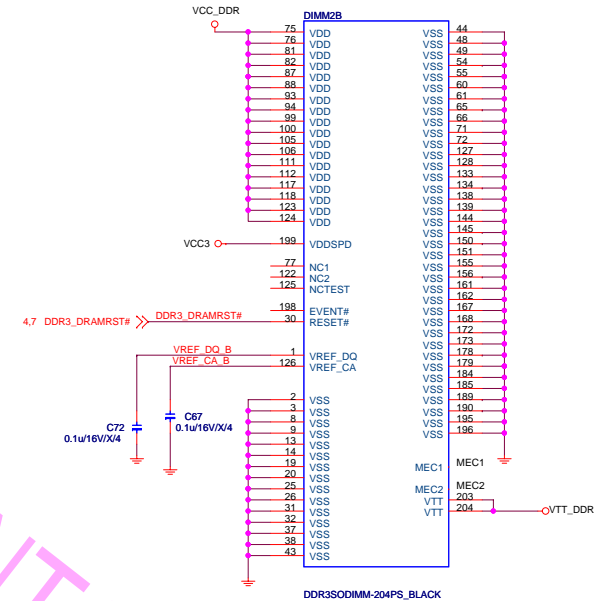
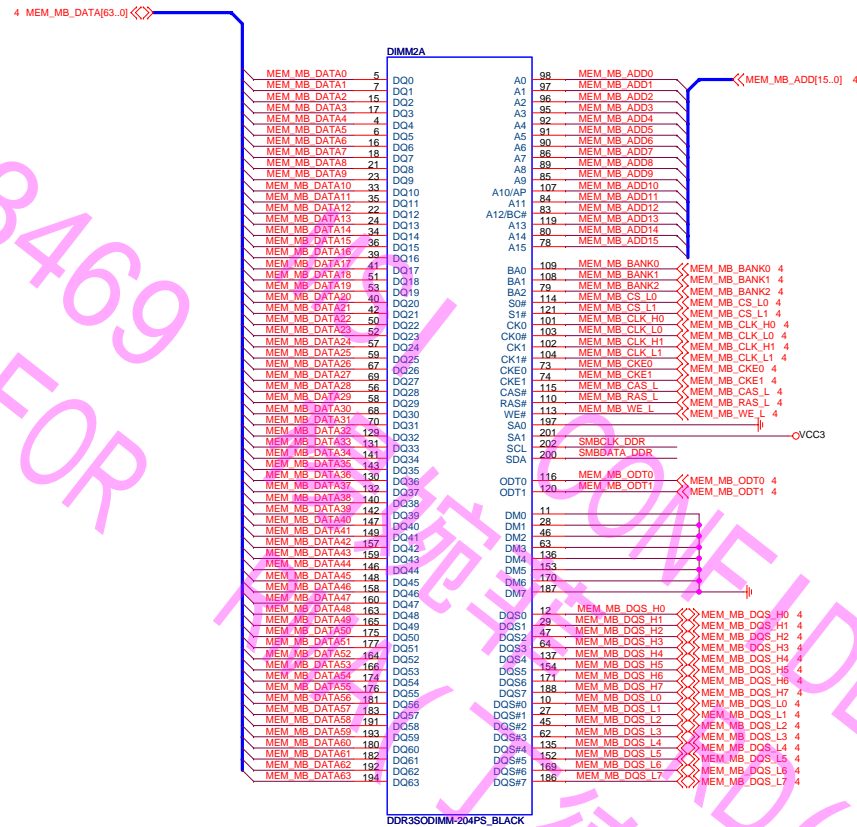
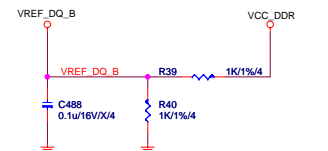
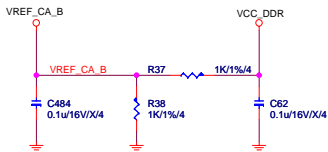
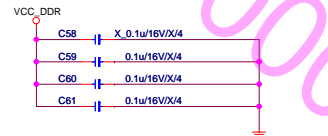


DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]



DDR3SODIMM-204PS_BLACK

SO_DDRIII DIMM_B0



```
DIMM2 (CHANNEL-B)  
ADDRESS = 1:0  
[SA1:SA0]
```

SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR

Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.
Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.



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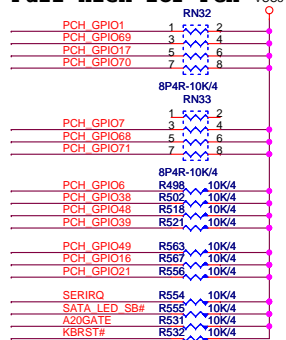
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Pull HIGH for PCH

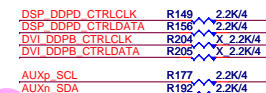


GPIO FOR BIOS



No VGA(pull down)

Enable VGA (CTRLCLK/DATA PULL HIGH)



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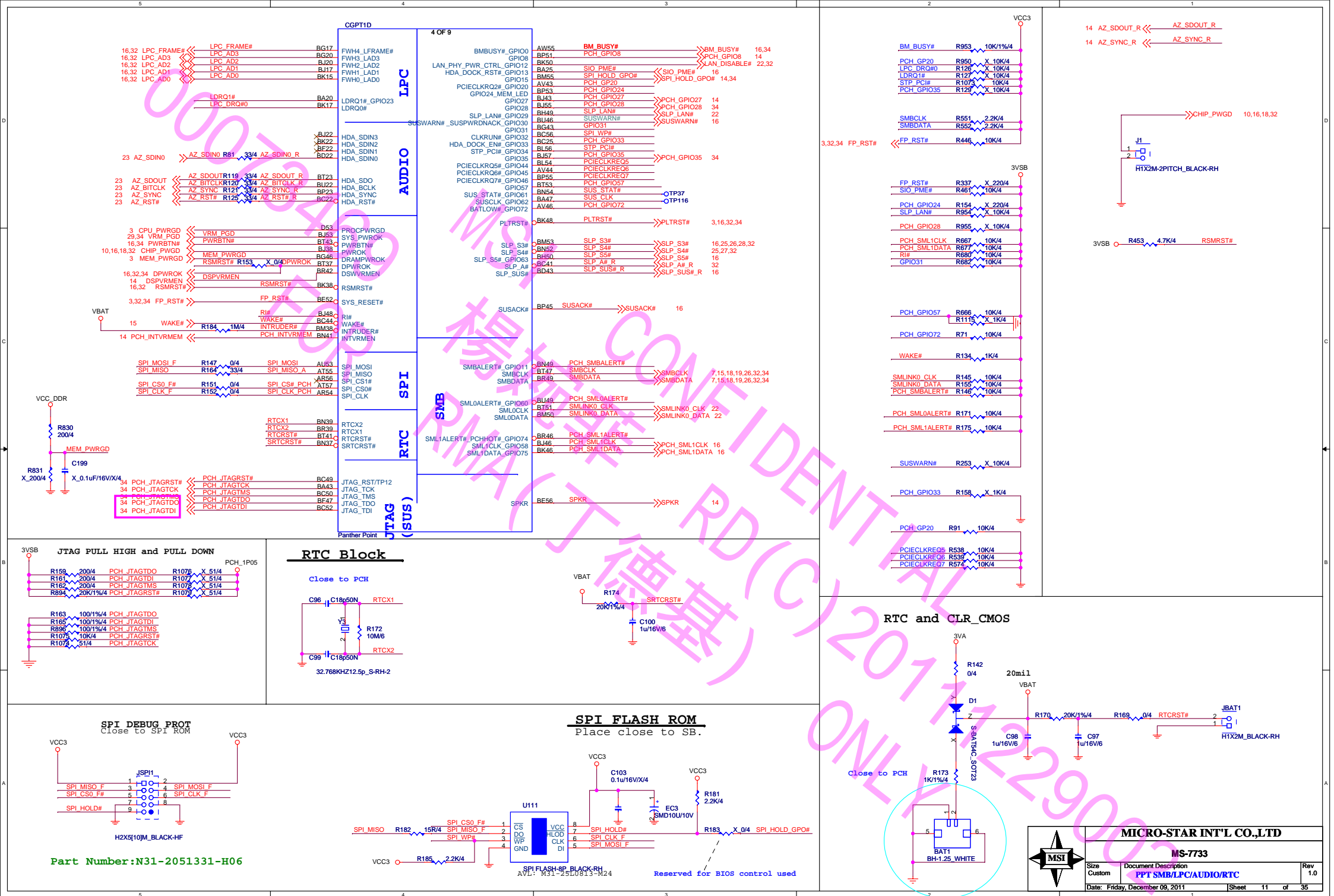
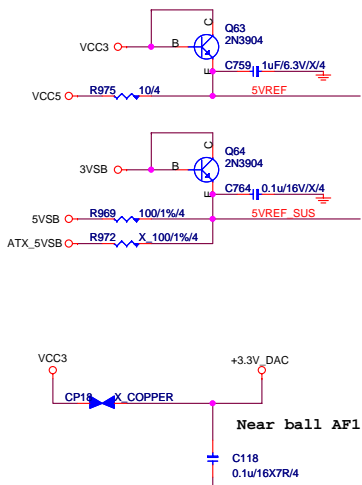


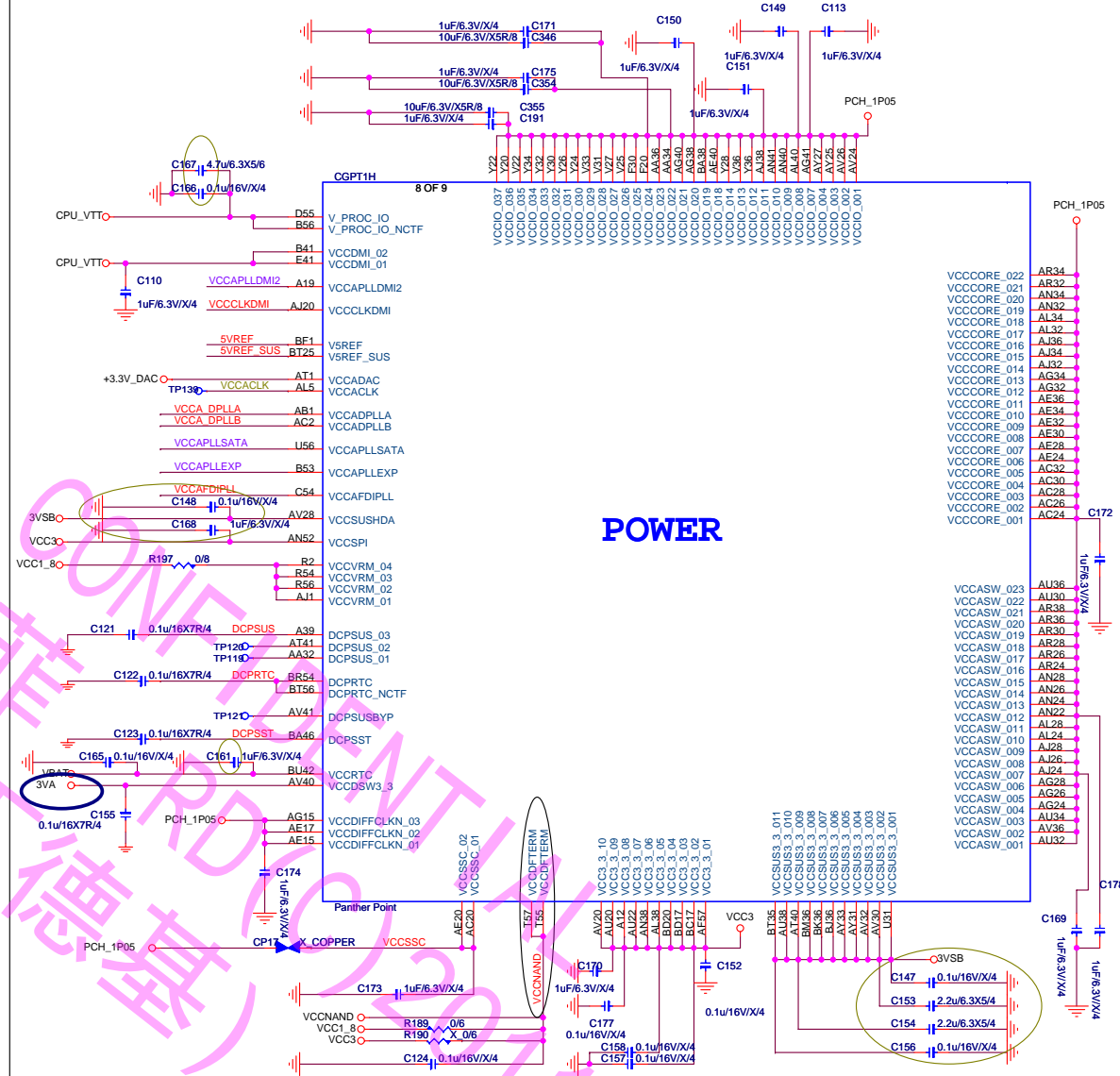
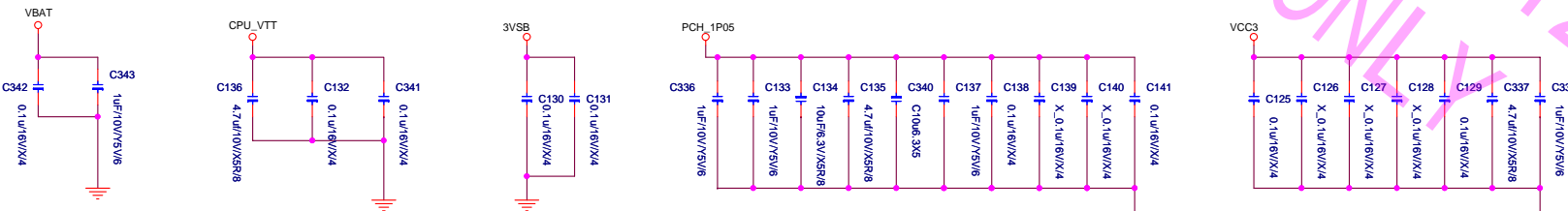
Table 3-7. VCCPLL Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µF	1	77mΩ	3.3nH	Output	North of processor - as close to RN keep-out as possible	1
10µF 0805 XSR	1	3mΩ	0.51nH	Output		1,2,3

5VREF & 5VREF_SUS Sequencing Circuit



PCH decoupling cap

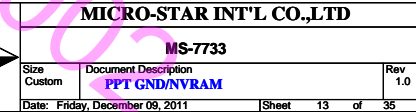
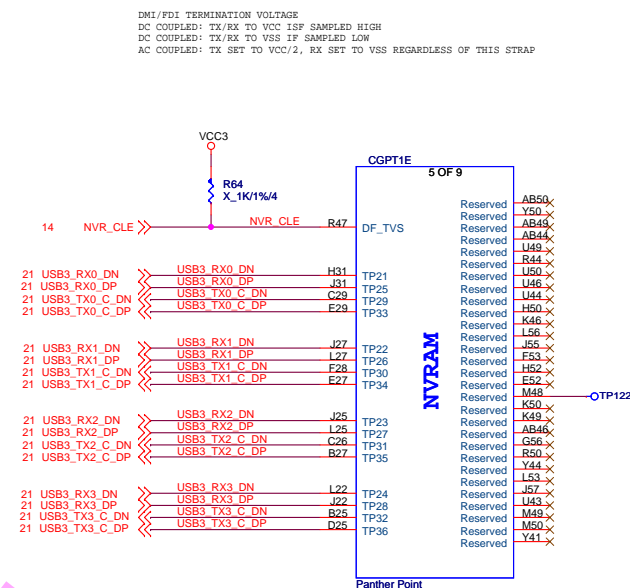


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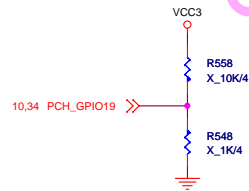
Size Custom	Document Description PPT POWER
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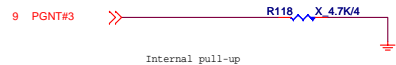


CP REQUIRED STRAPS

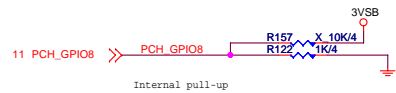
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating



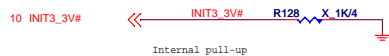
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up

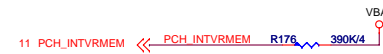


GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

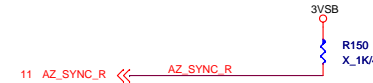


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

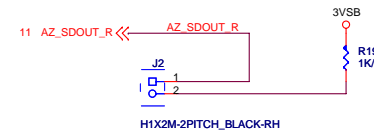
When these vltageregulators are enabled, the
integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V
regulators. Must beconnected even when not supporting DSW.



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

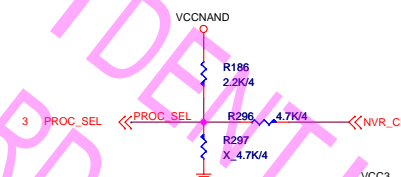


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW

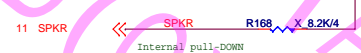
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



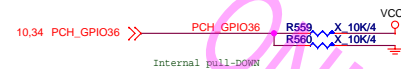
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
(Sandy Bridge R186 2.2K ohm,R296 0ohm Stuff; R297 empty)
(Ivy Bridge R186 2.2K ohm,R296 1Kohm Stuff; R297 empty)
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP
(Ivy Bridge: R186,R296 empty; R297 Stuff)



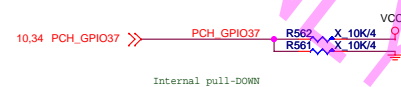
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used,require a weak pull-up(8.2k-10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high

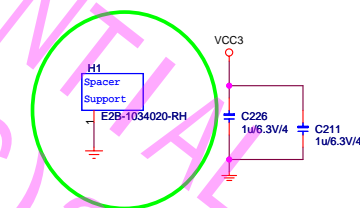
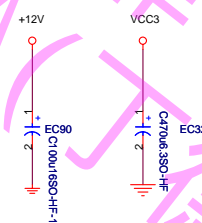
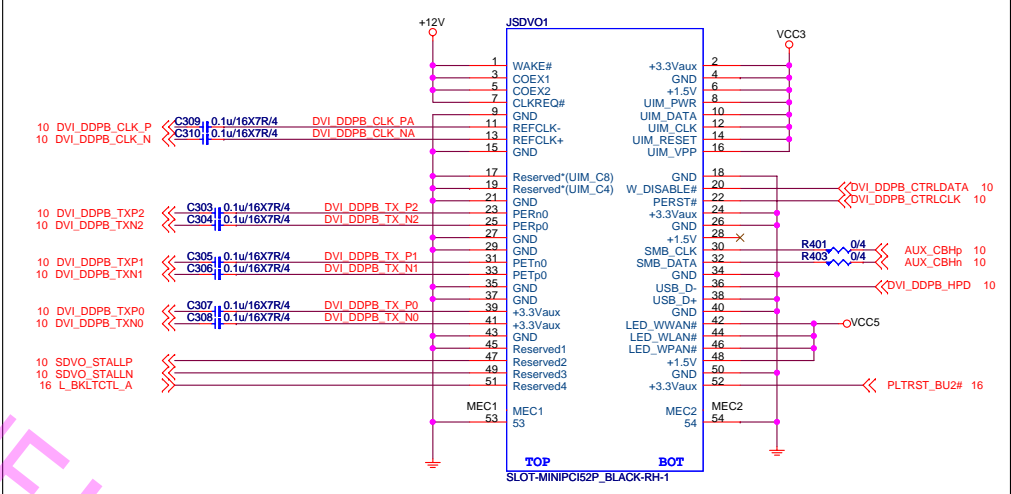


Cougar point EDS PAGE:93 This signal should not be pull high



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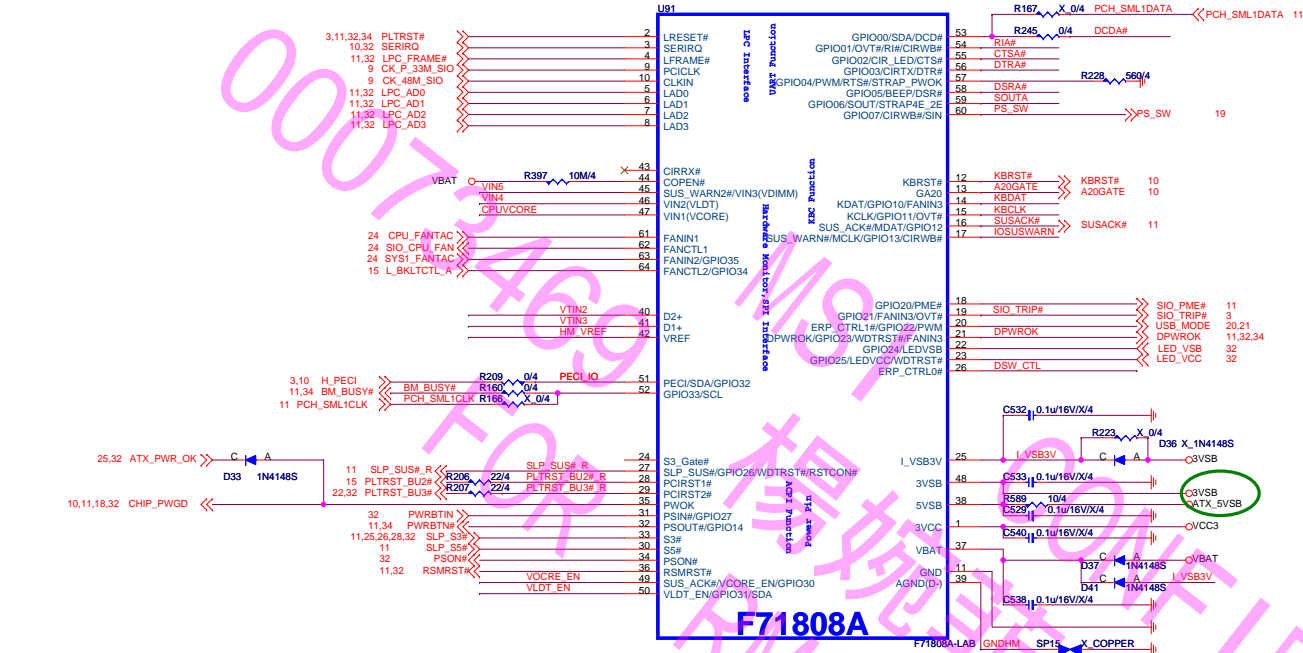
SDVO connect



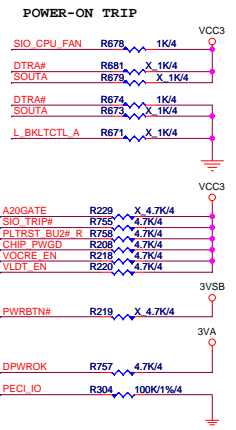
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Size Custom	Document Description PCIEX1 Slot / SDVO connect	Rev 1.0
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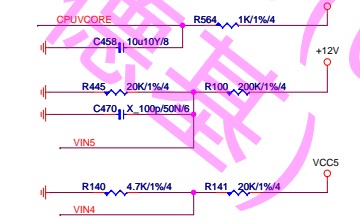


LPC I/O STRAPPING RESISTOR

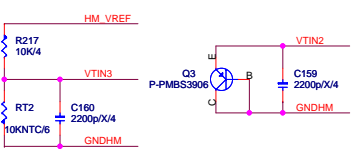


PIN	Function	NET Name	HI	LO
64	L_BKLTCTL_A	FANCTL2	PWM FAN	LINEAR FAN
62	SIO_CPU_FAN	FANCTL1	PWM FAN	NOT SUPPORT LINEAR FAN
56	DTRA#	FAN40_100	FAN SPEED DUTY:40%	FAN SPEED DUTY:100%
59	STRAP4E_2E	Config 4E/2E	4E(DEFAULT)	2E
57	STRAP_PWOK	STRAP_PWOK	INTEL (DEFAULT)	AMD

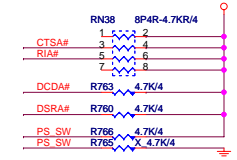
Voltage Detect



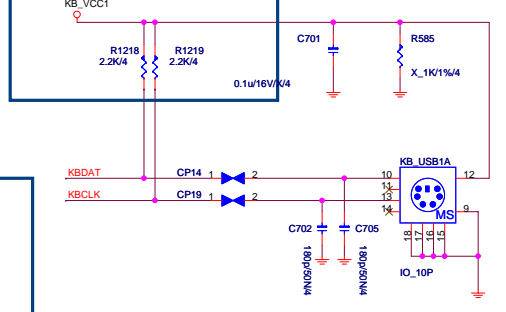
Thermal Resistor



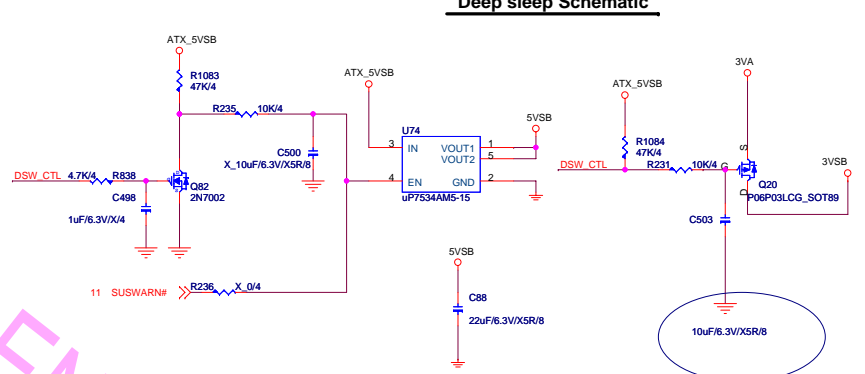
SERIAL PORT 1



KB MOSE ADD USBX2



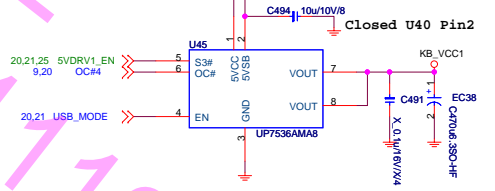
5VSB Power Switch



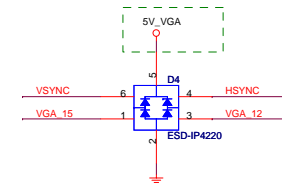
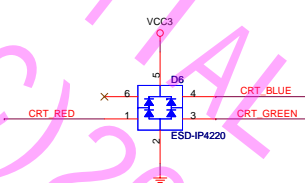
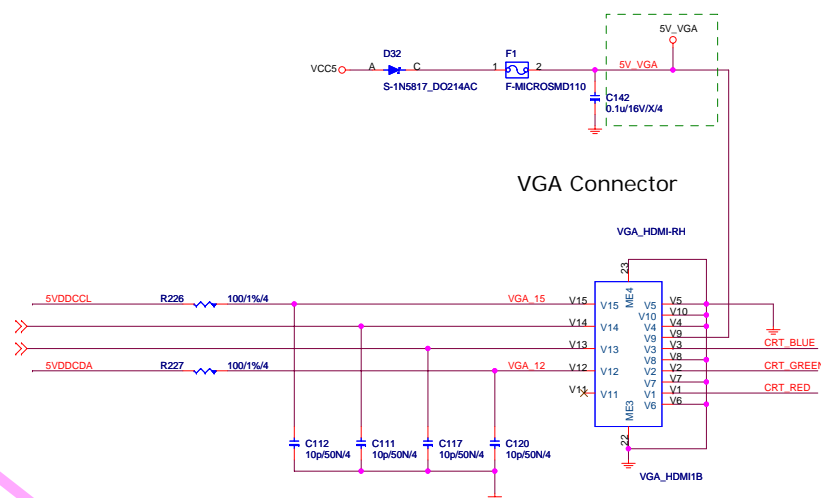
Deep sleep Schematic


KB MOSE POWER

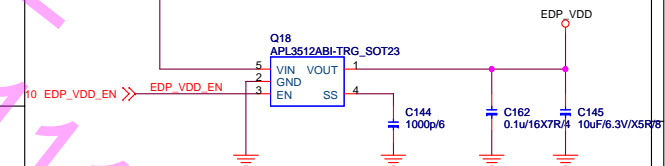
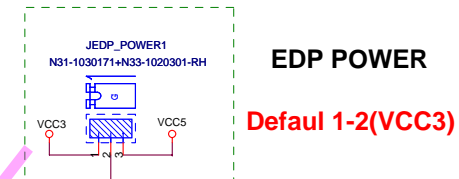
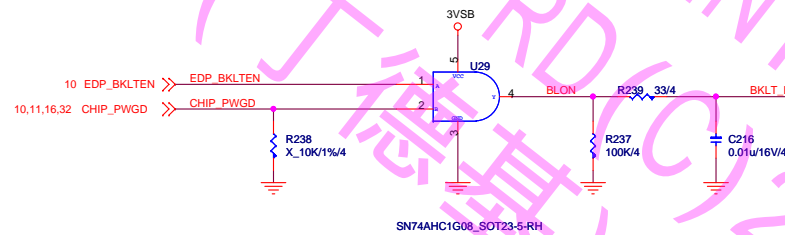
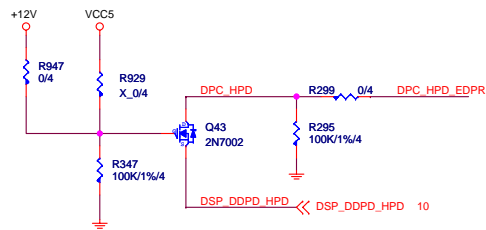
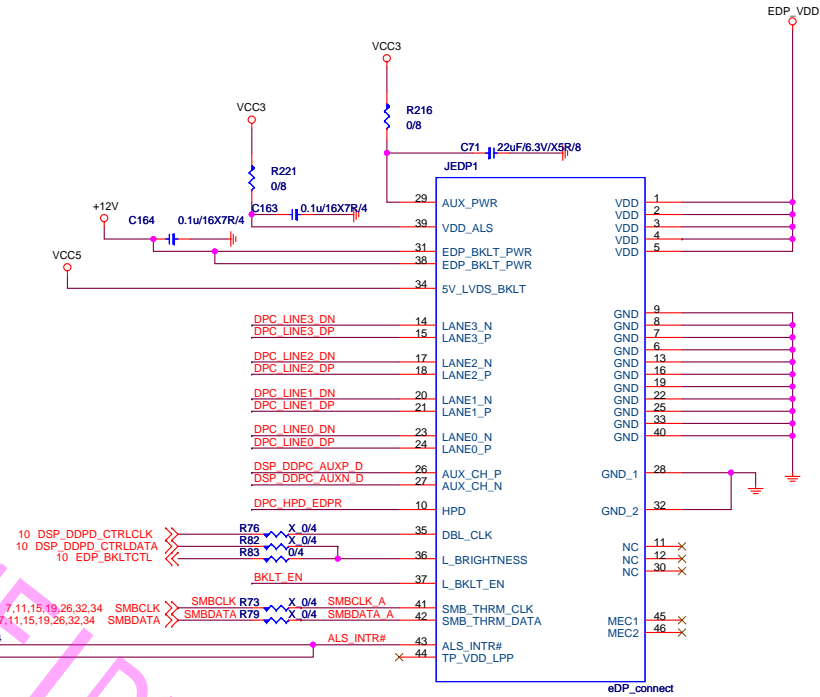
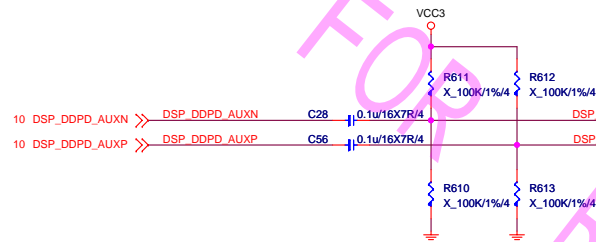
NEAR CONNECTOR



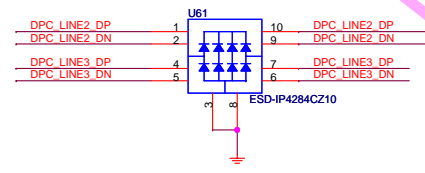
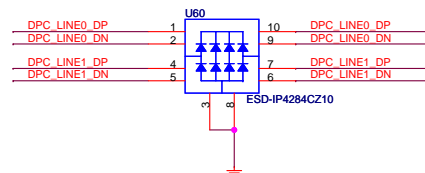
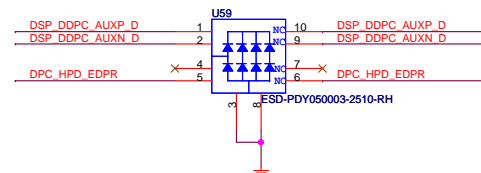
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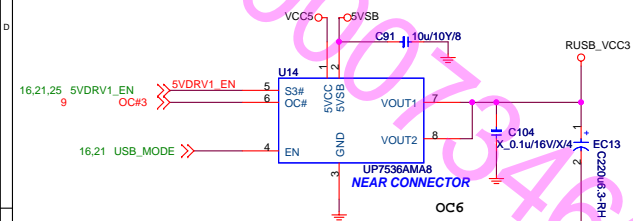


For EMI

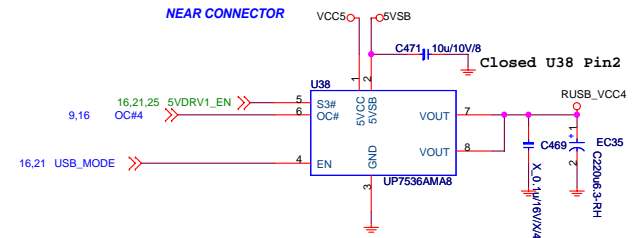
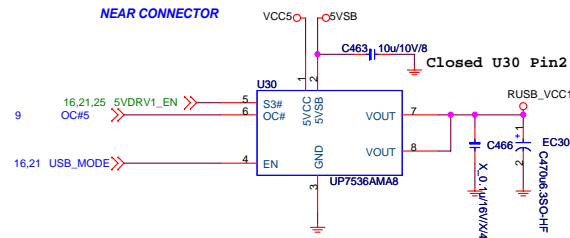


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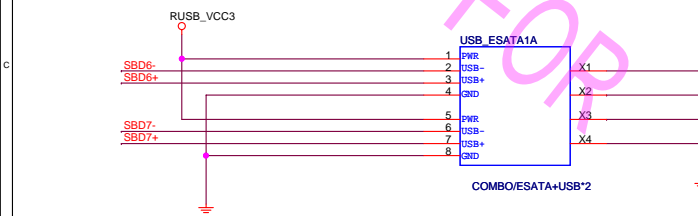
NEAR USB PORT 12,13 (ESATA)



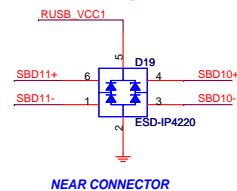
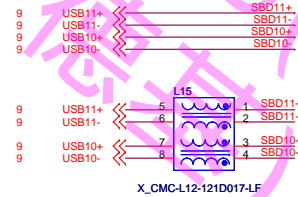
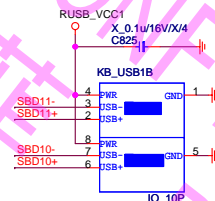
Rear USB Connector



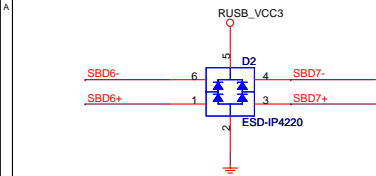
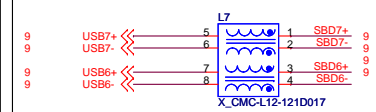
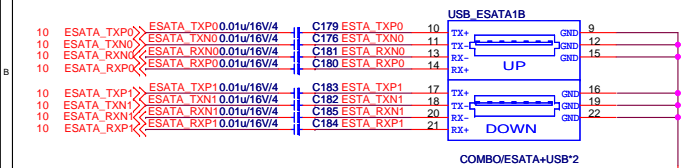
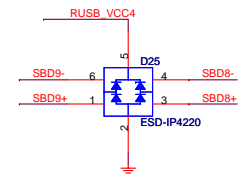
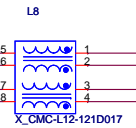
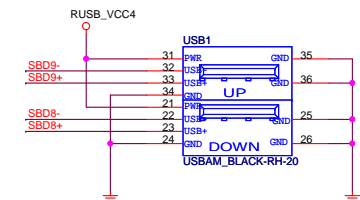
NEAR CONNECTOR



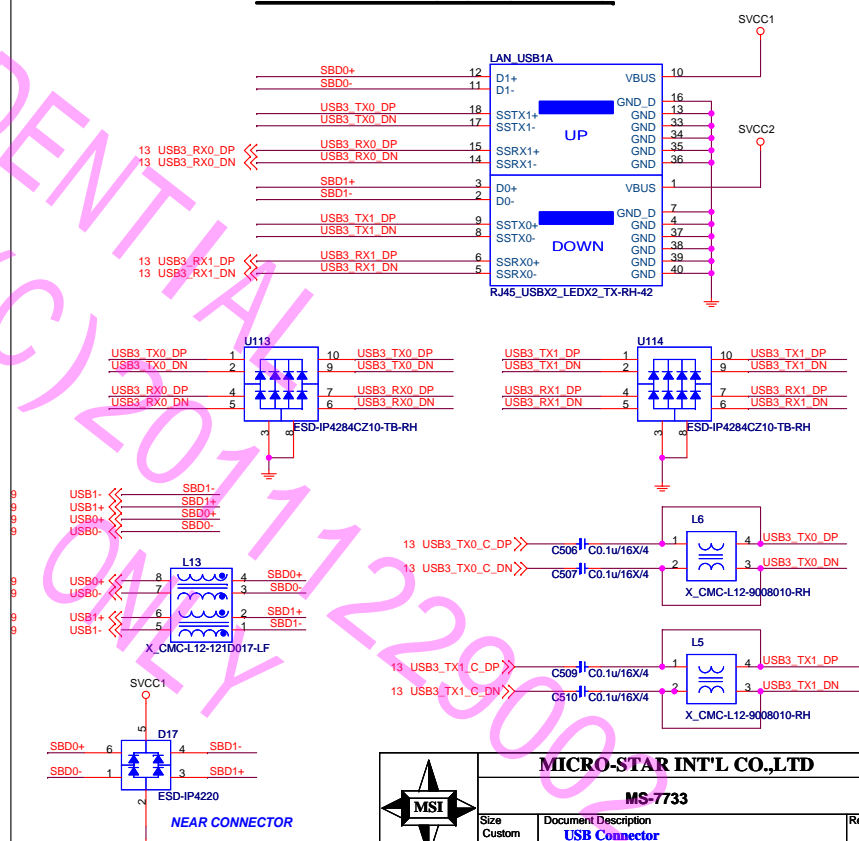
REAR USB PS2&USBX2 PORT(6,7)



NEAR CONNECTOR



NEAR CONNECTOR VCC5 5VSB



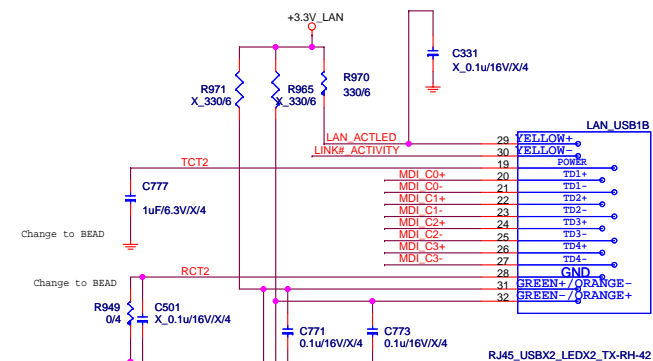
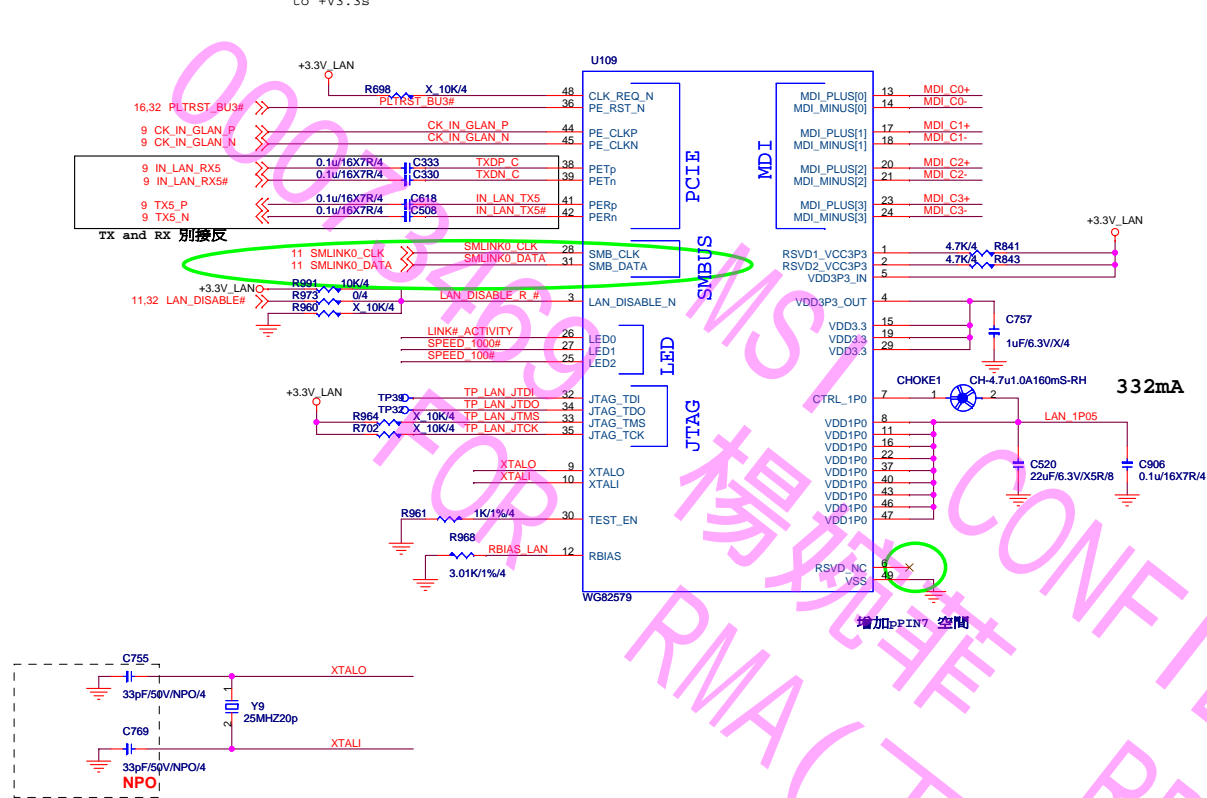
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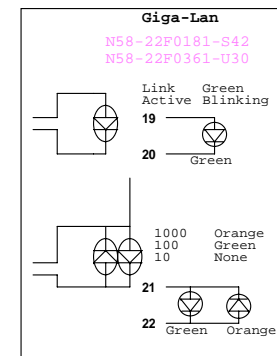
Size Custom	Document Description USB Connector	Rev 1.0
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$$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} \times R_2$$

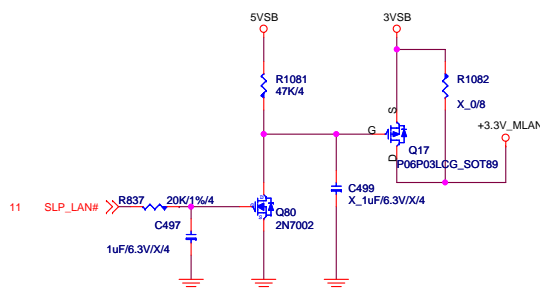
If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,
the CLK_REQ_N pull-up resistor should be connected
to +V3.3s



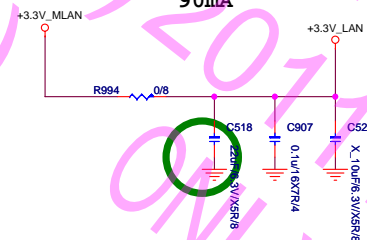
LAN新燈號的部分還在申請
N58-22F0541-F02



+3.3V LAN



90mA

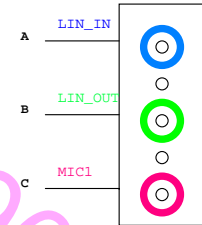
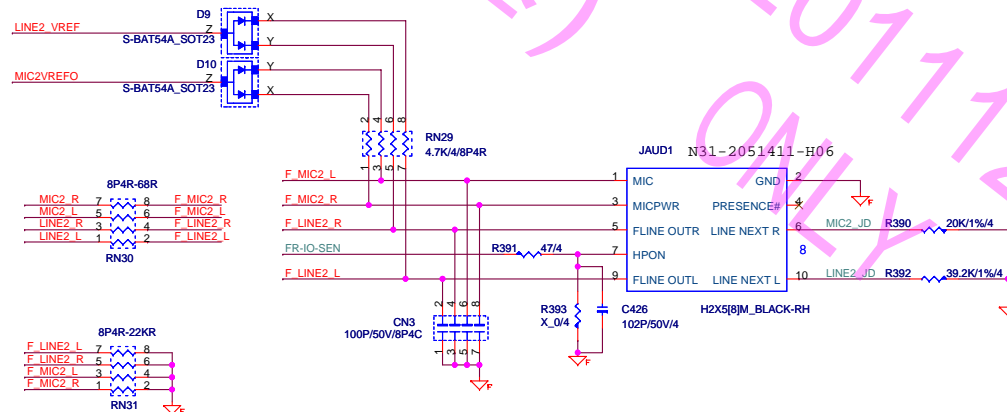
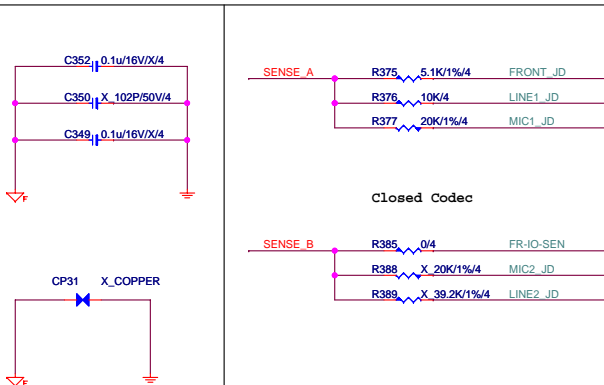
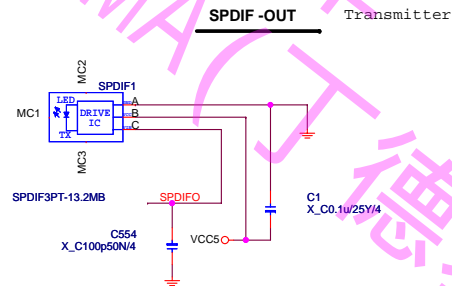
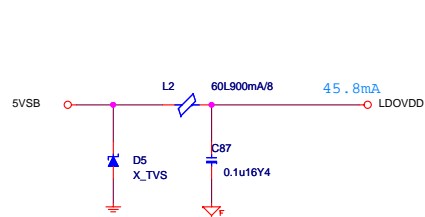
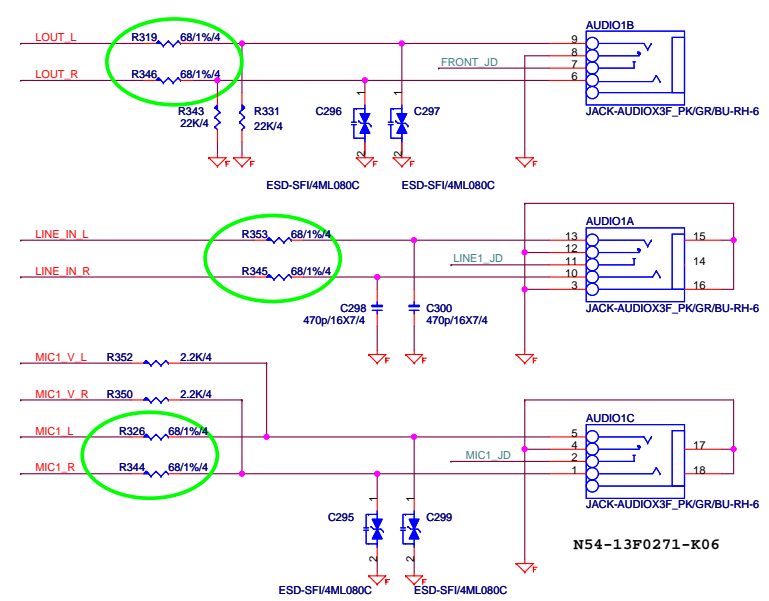
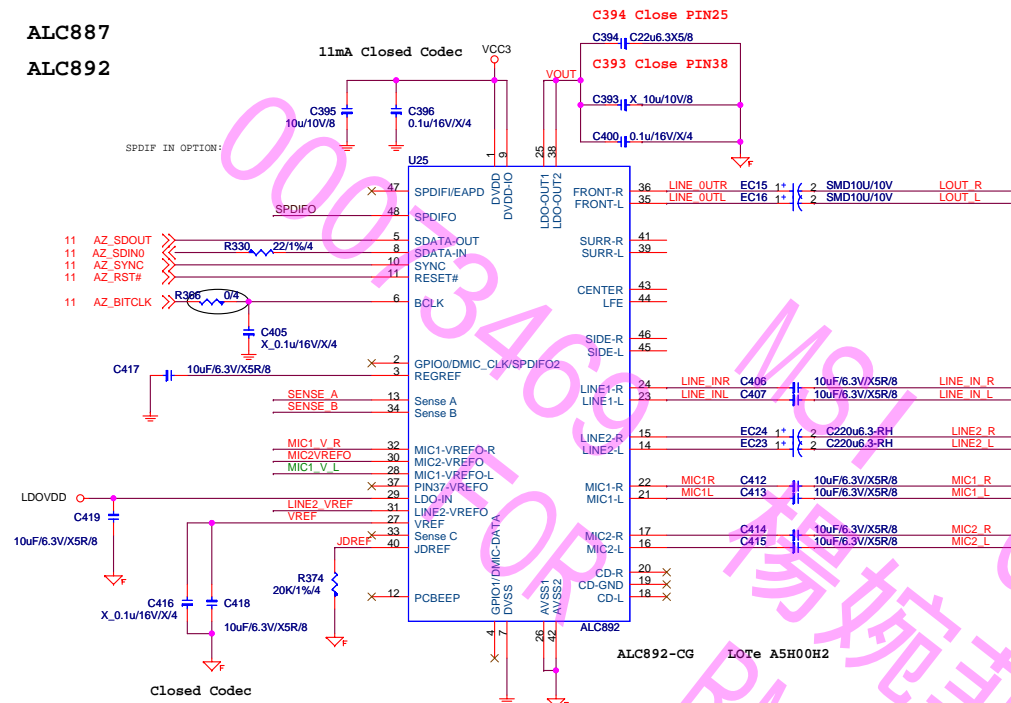


Note: These caps closed to PHY



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ALC892

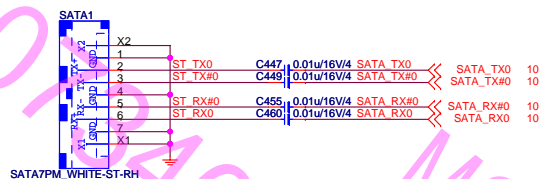


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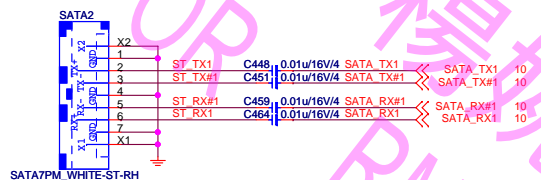
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Size Custom	Document Description Audio Codec ALC892/887	Rev 1.0
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SATA 3.0



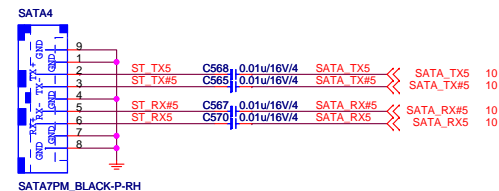
SATA 3.0



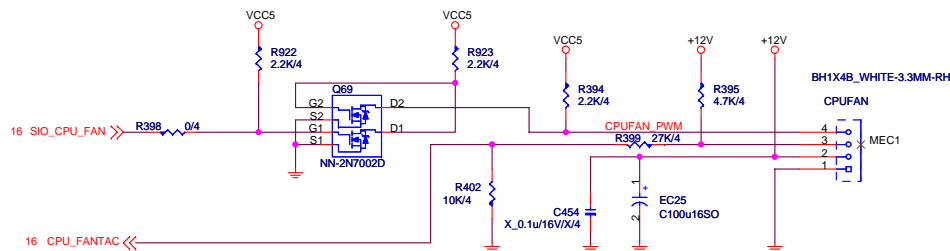
SATA 2.0



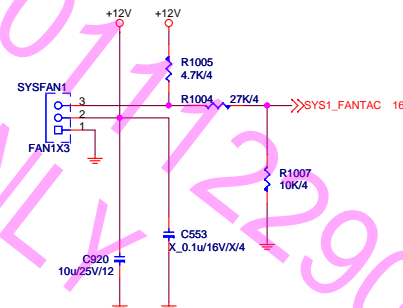
SATA 2.0



CPU FAN-COUNTROL CIRCUIT



SYS FAN CIRCUIT

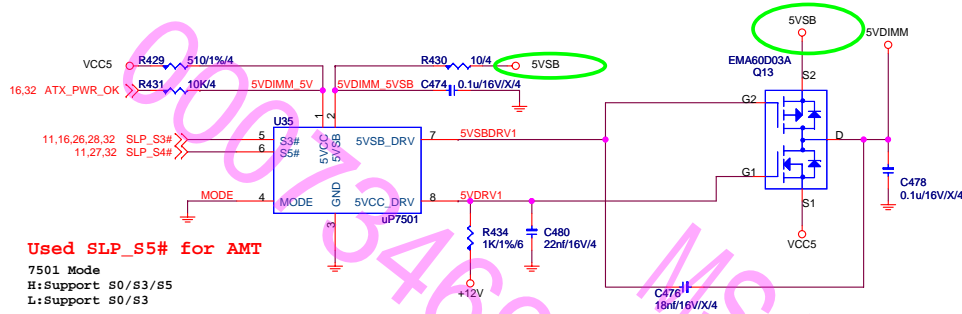


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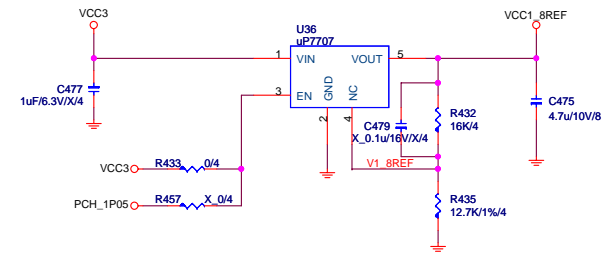
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Custom	SATA / FAN Control	1.0
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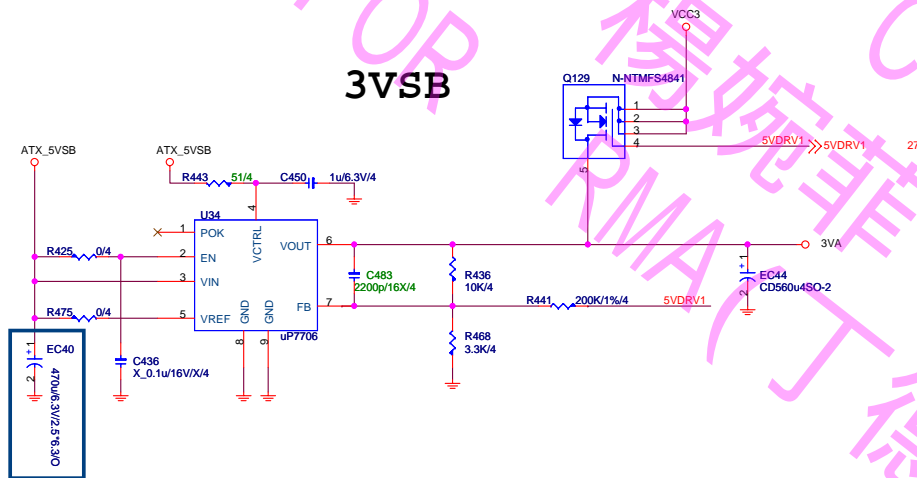
5VDIMM FOR DDR



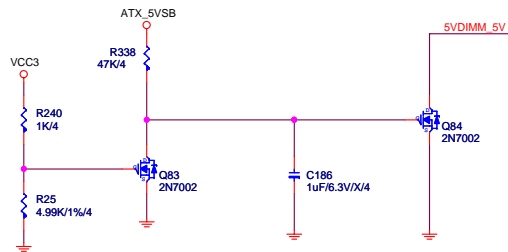
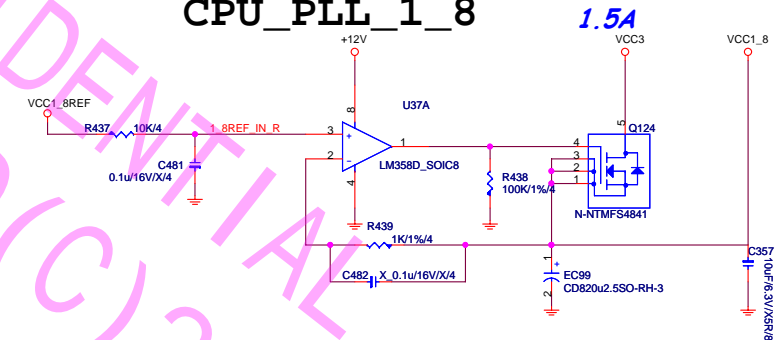
VCC1_8REF



3VSB

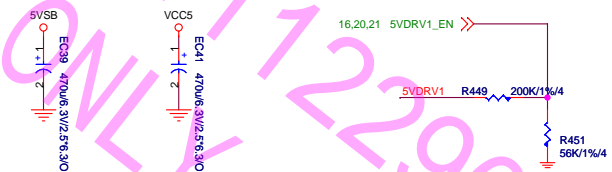


CPU_PLL_1_8



For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

USB MODE

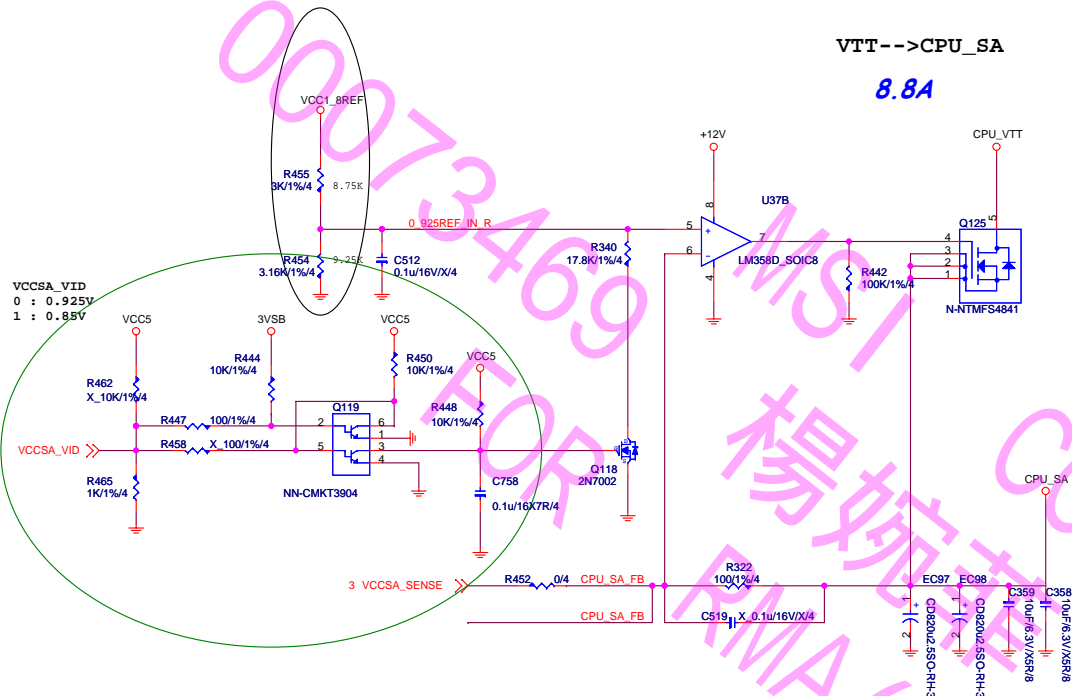


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CPU_SA Power

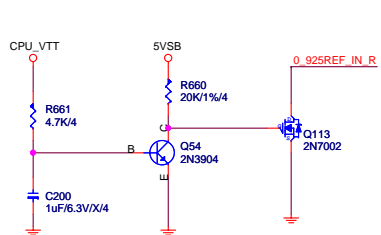


page 5

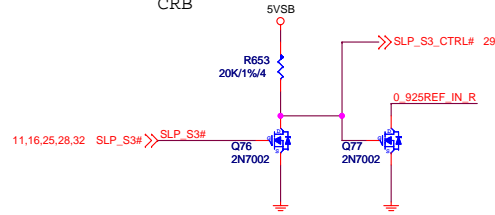
Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560uF	1	7mΩ	1.4nH	Output	As close to RM loop-out as possible	1
10uF 0805 XSR	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1,2

Waiting CPU_VTT Ready



CRB



CP Power

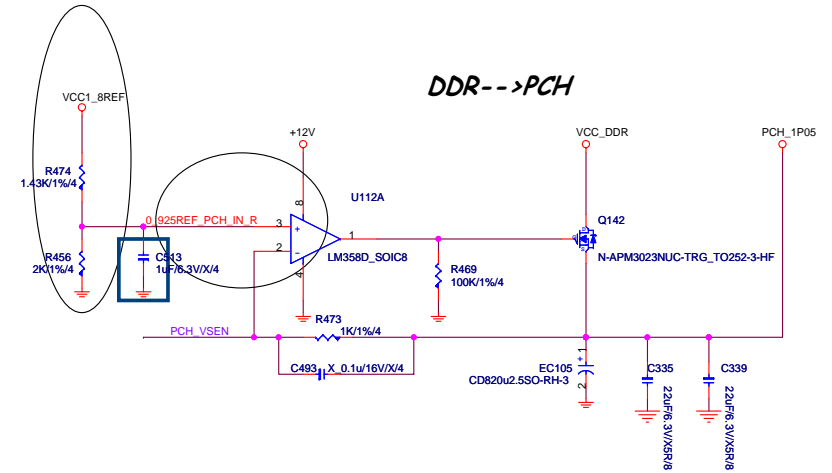
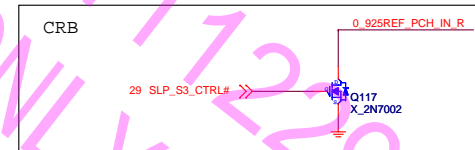
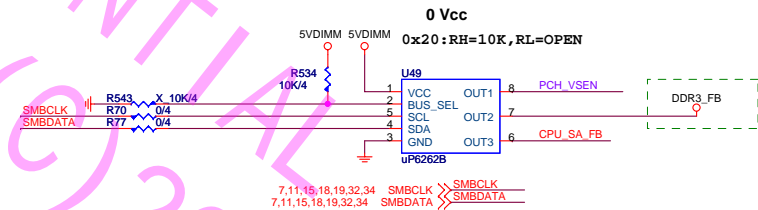


Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

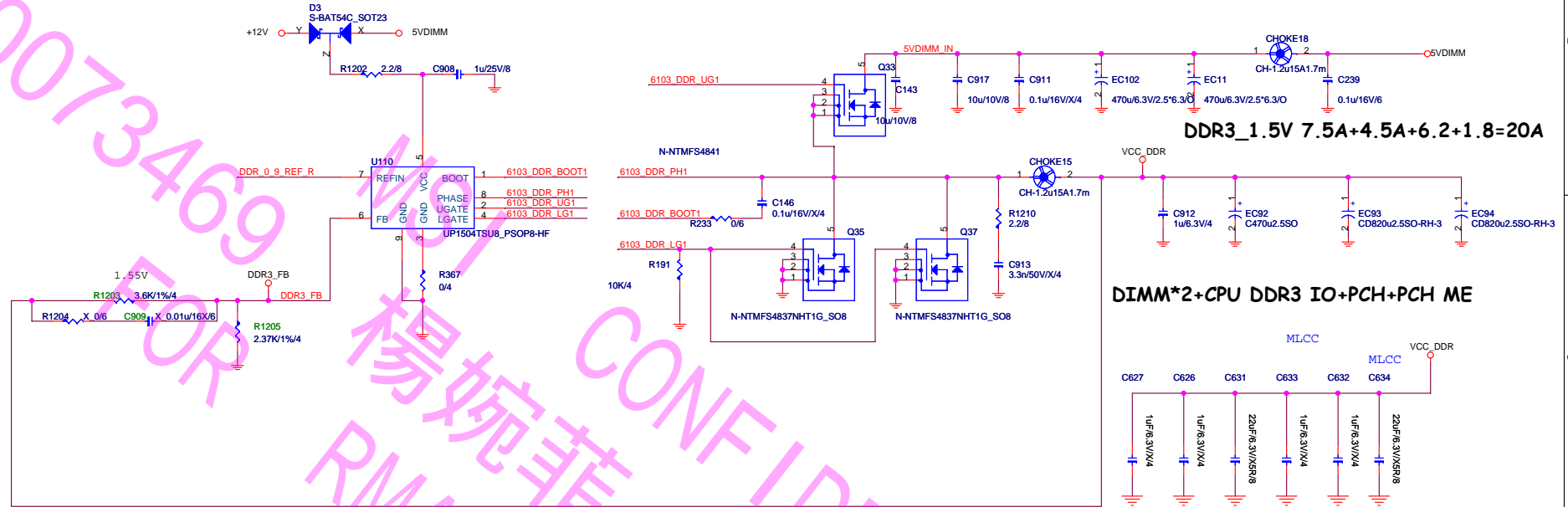
Bulk Decoupling Location	Qty x uF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non-AMT sku)	1x560uF 2x 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different than those shown.

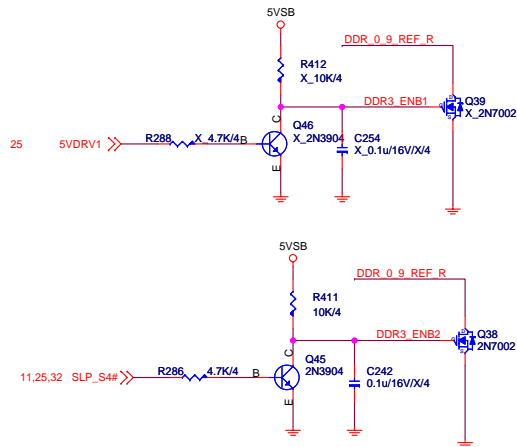
UPI VOLTAGE CONSOLE



DDR Power



Intel Power on for 5v droop issue



Meet Intel Power Down Sequence

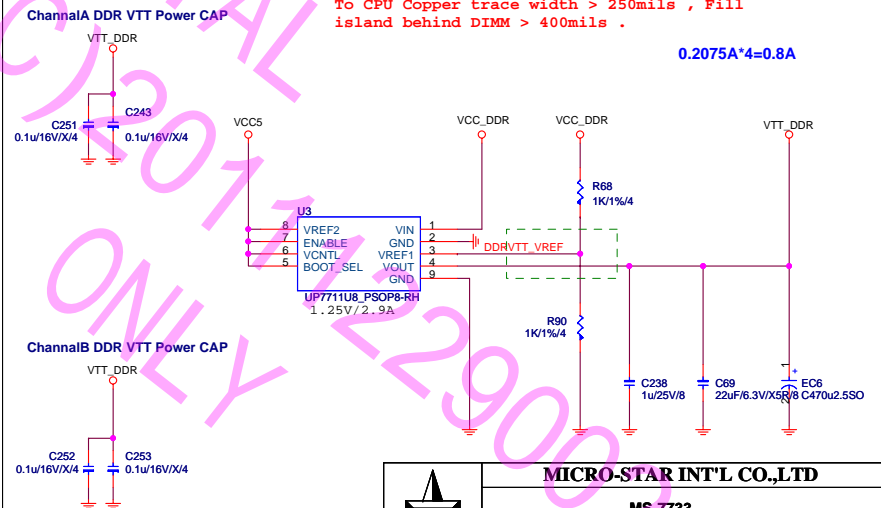
Table 3-11. VDDQ Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 1000uF	3	5mΩ	1.8nH	Output	Close to power pins	1, 2
22uF 0805 XSR	9	5mΩ	0.55nH	Output		

DDR VTT Power

To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils.

$$0.2075A \times 4 = 0.8A$$

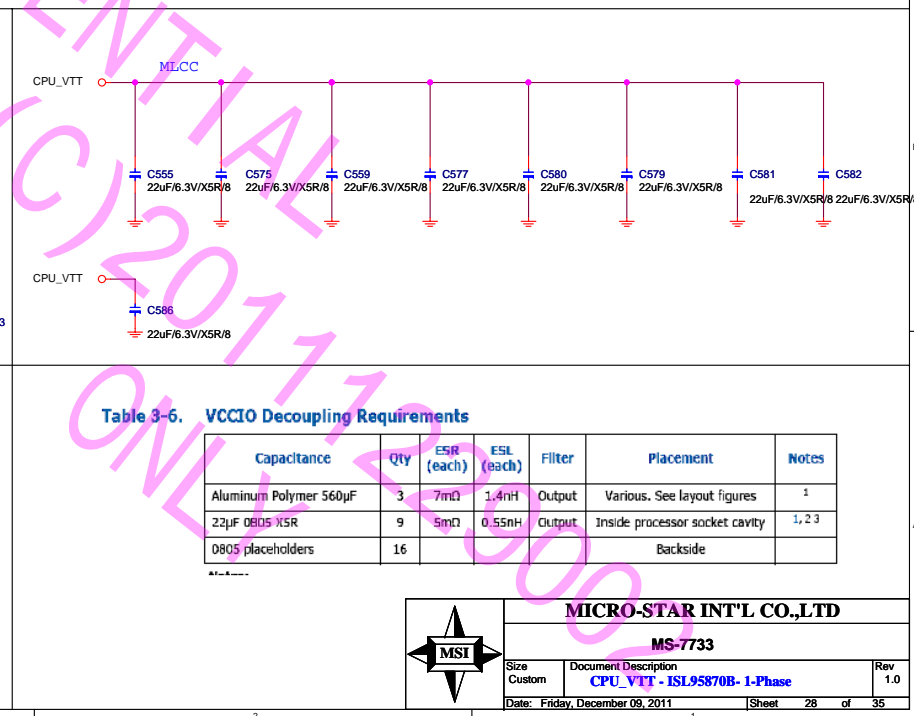
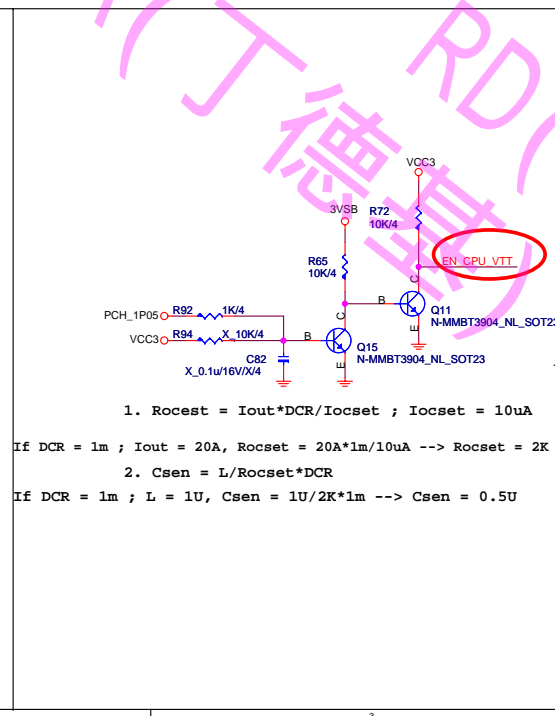
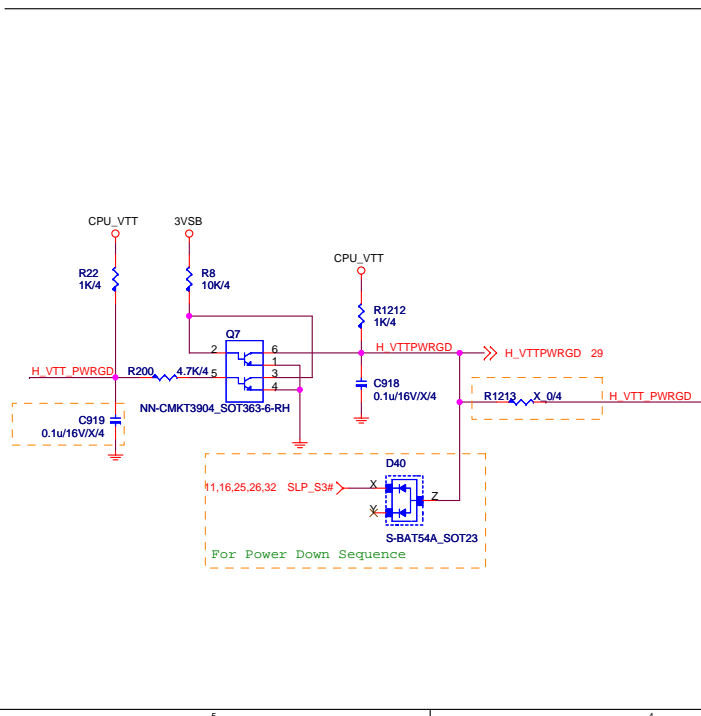
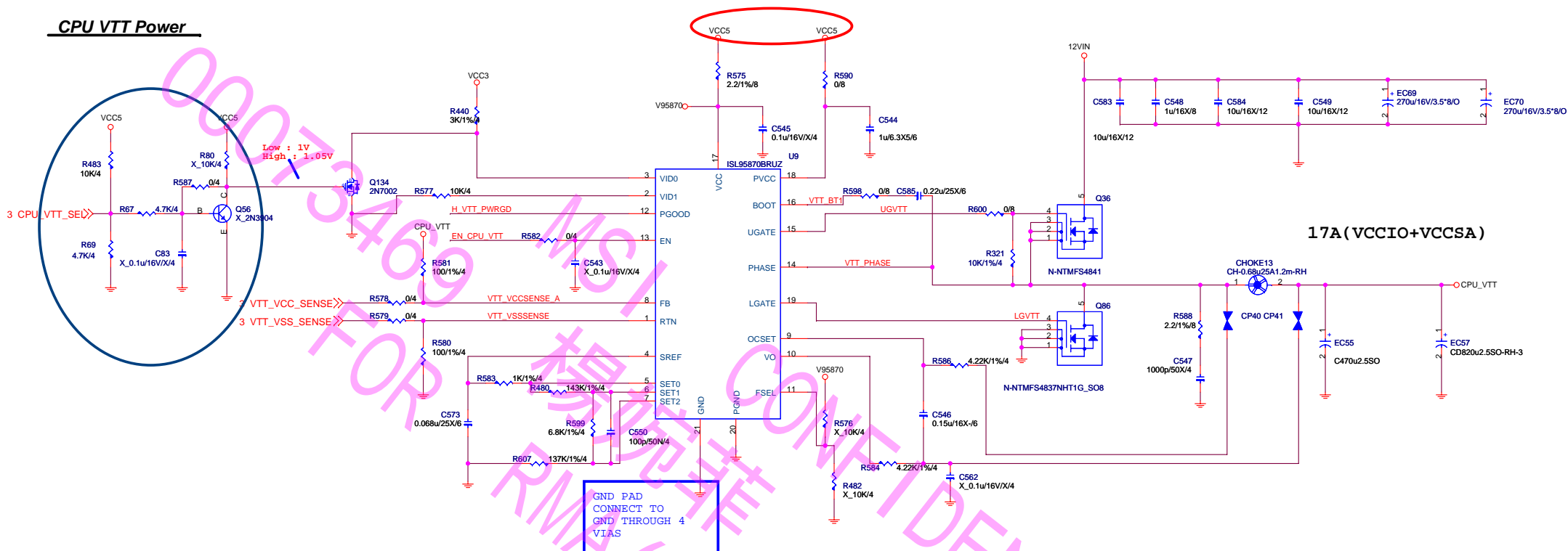


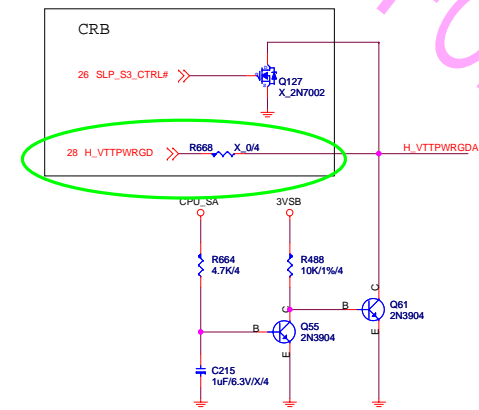
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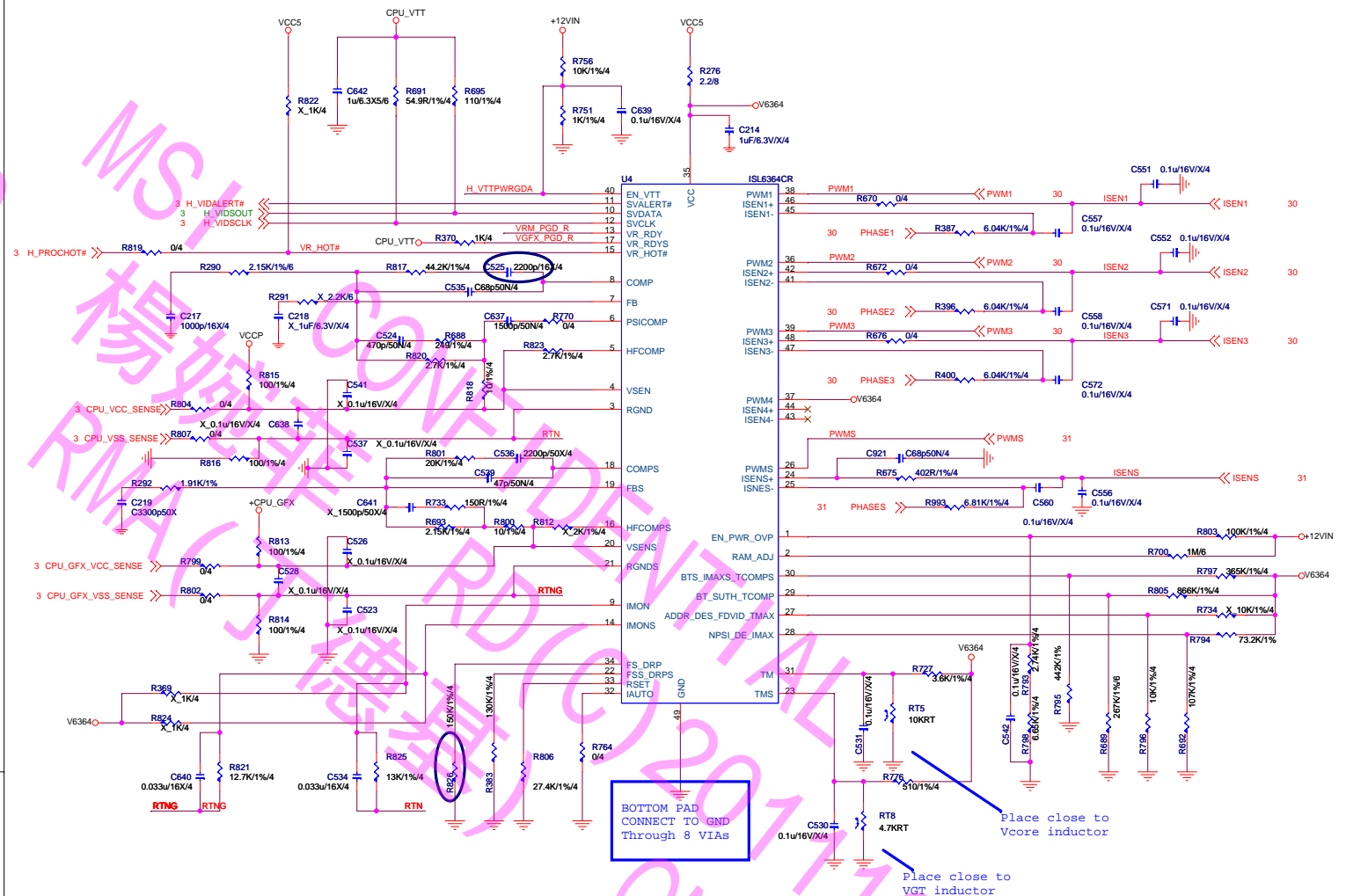
Size	Document Description	Rev
Custom	DDR POWER-UP6103 1-Phase	1.0
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CPU VTT Power



[illegible]

VCCAXG MAX: 35A

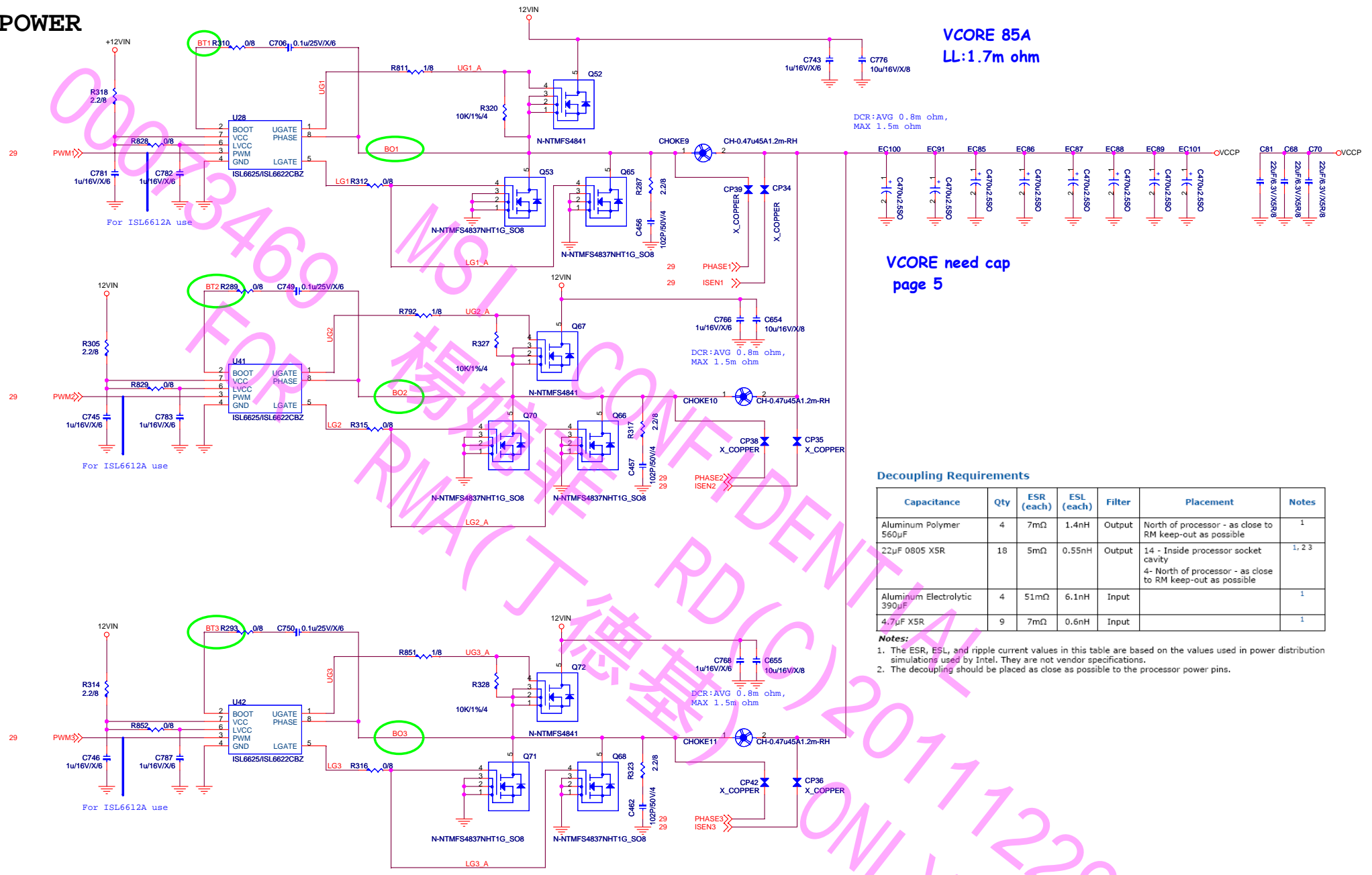


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VCCP POWER

VCORE 85A
LL:1.7m ohm



VCORE need cap
page 5

Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560μF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22μF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2, 3
Aluminum Electrolytic 390μF	4	51mΩ	6.1nH	Input		1
4.7μF X5R	9	7mΩ	0.6nH	Input		1

Notes:
1. The ESR, ESL, and ripple current values in this table are based on the values used in power distribution simulations used by Intel. They are not vendor specifications.
2. The decoupling should be placed as close as possible to the processor power pins.

GFX POWER

VCCAXG SVID:25A TDC:35A

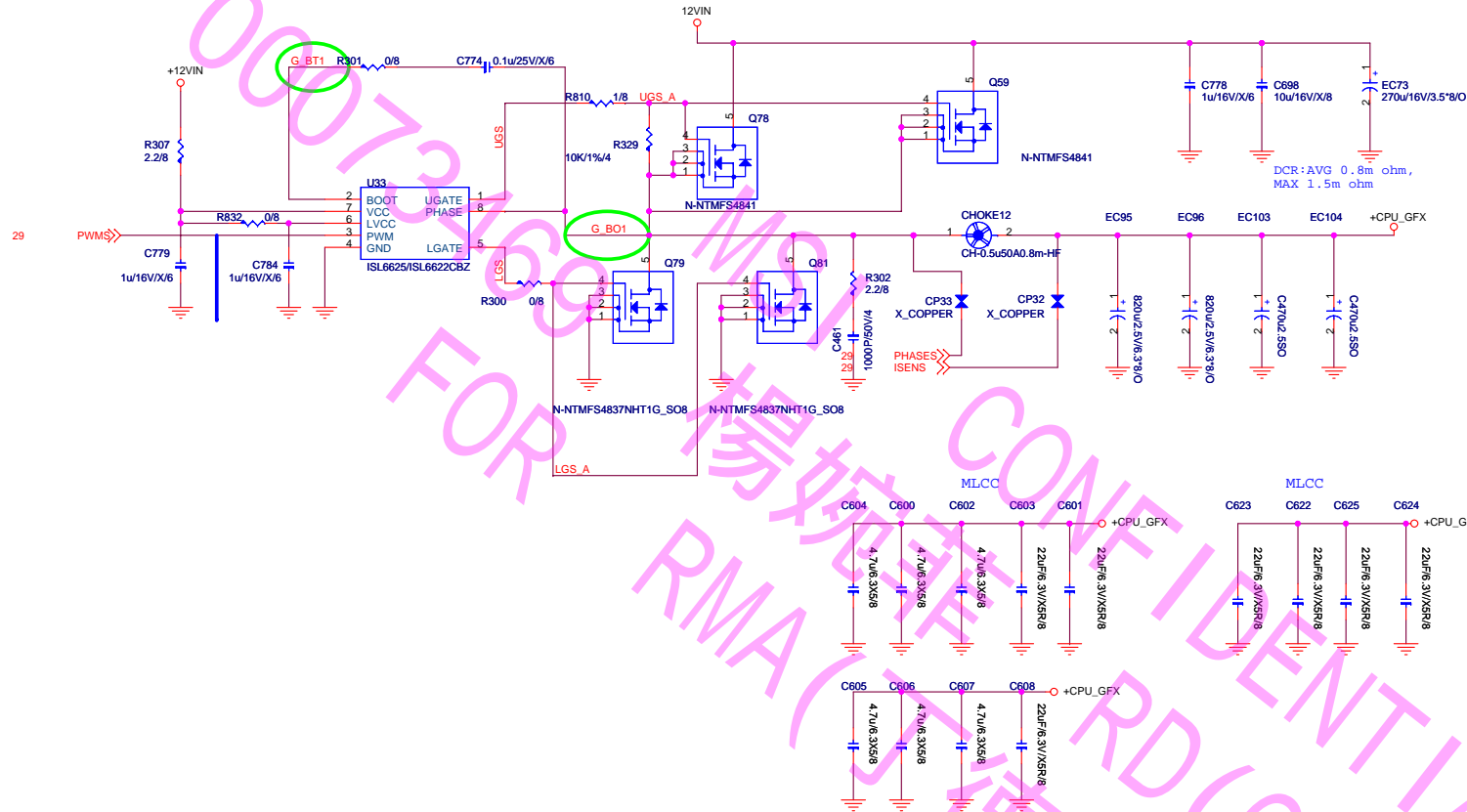


Table 3-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RJM keep-out as possible	1
22µF 0805 XSR	6	5mΩ	0.55nH	Output	4 - Inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF XSR	3	7mΩ	0.6nH	Input		1

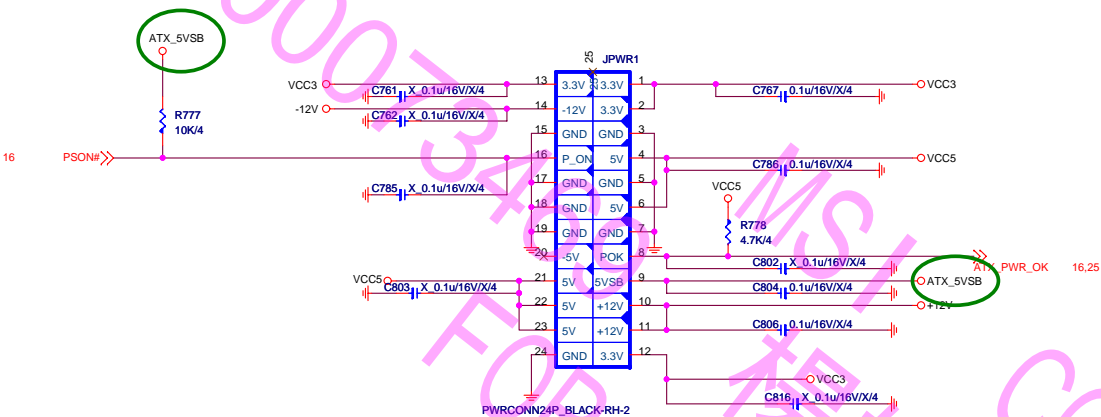


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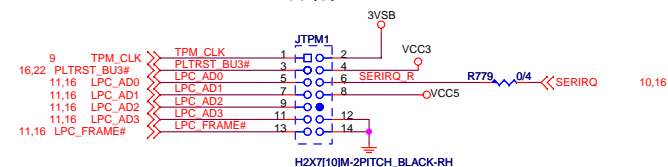
ATX POWER CONNECTOR



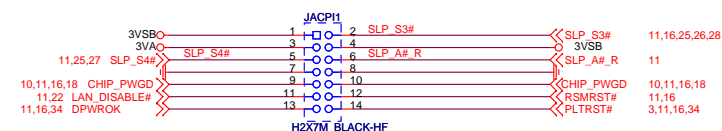
SMBUS PIN HEADER



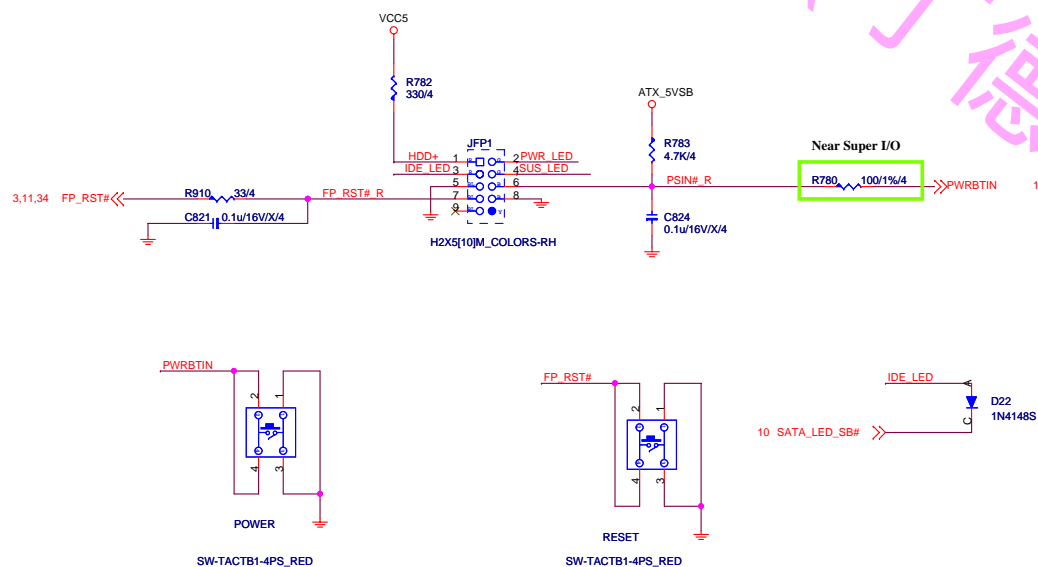
TPM



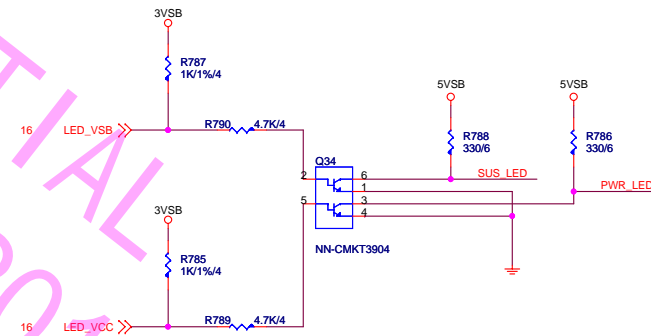
FOR INTEL TEST



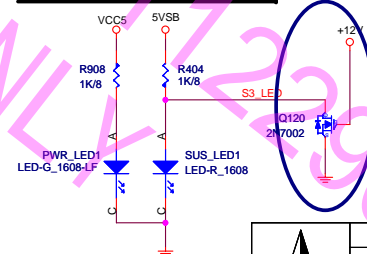
FRONT PANNEL



LED (for Fintek 71882)



POWER LED(S0/S5)



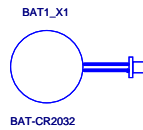
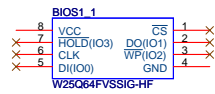
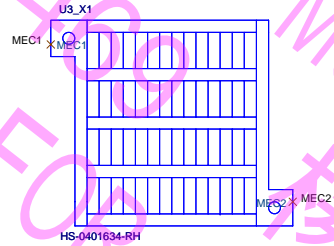
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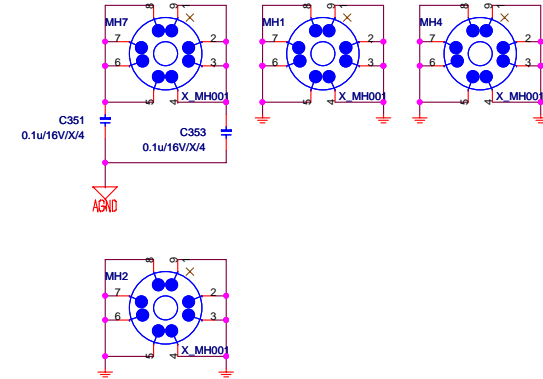
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Custom	ATX F_Panel/EMI/TPM	1.0
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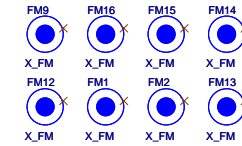
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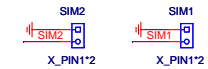
Mounting Holes



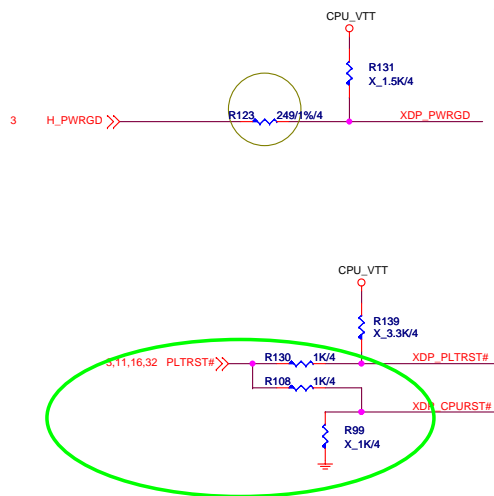
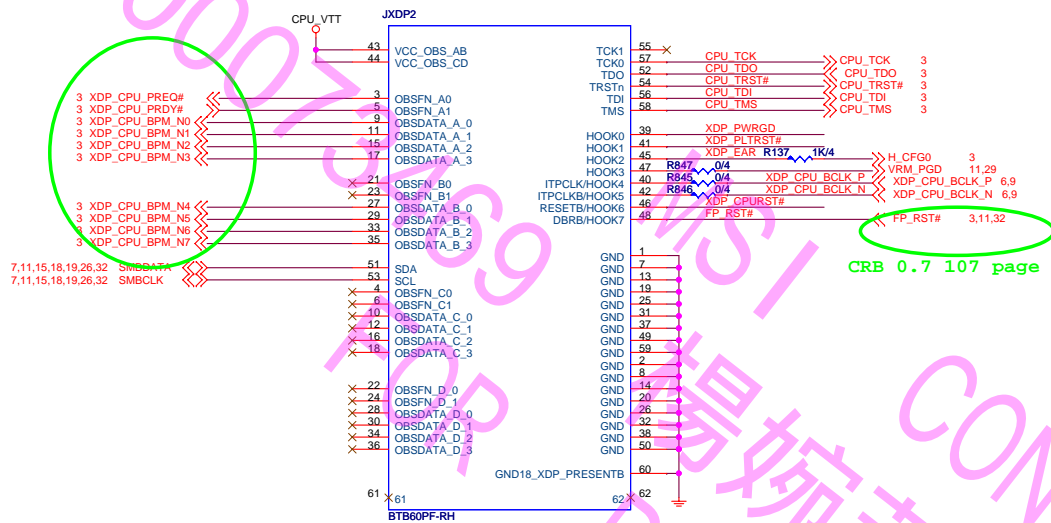
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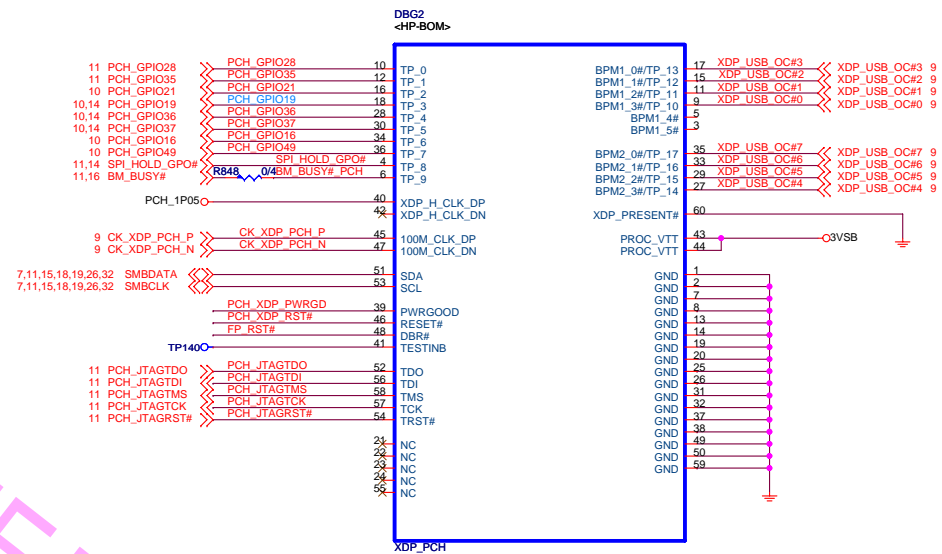
Simulation



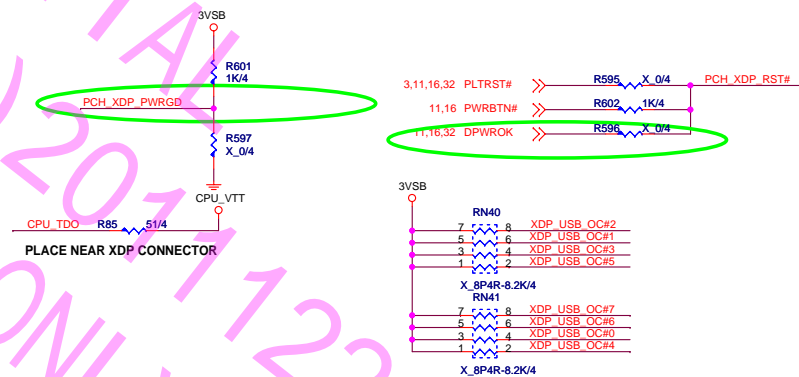
Reserve debug port 5020



PCH XDP



PCH XDP PWRGD/RESET



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7733-0A----->0B History

Schematic History

1.add two 7002 MOS to let 5VDIMM_5V wait VCC3 Reson:The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but VCC3 not ready and let the 3VSB sequence fail.[page 25]

2.add R587,R483 Reson:CPU_VTT_SELECT conform to right voltage level.[page 28]

3.change Q120.G to +12V . Reason:S5 to S0,let SUS_LED to close.[page 32]

4.It add one phase in VRM,and it change two phase to three phase.[page 30]

5.It add 3VA voltage in JACPI1 connector.[page 32]

6.It change pin3 to SMBDATA of JSMB1.[page 32]

7.It change pin2 to GND of JSMB1.[page 32]

8.It change AUDIO CODE ALC889 to ALC892 of U25.[page 23]

9.It add C495,C496,C502,C505,C506,C507,C509,C510 of USB 3.0 TX.[page 21]

10.It add L3;L4;L5;L6 of USB 3.0 signal.[page 21]

7733-0B----->0C History

Schematic History

1.Add JEDP_POWER1 for EDP POWER voltage level.(It is 15.6 inch monitor of VCC3 voltage level.It is 21.5 inch monitor of VCC5 voltage level) [page 18]

2.It don't contact in U3 PIN3 and PIN4. [page 27]

3.It change NMOS Q135 to Q142. [page 26]

7733-0C----->0D History

Schematic History

1.PCIEX1 change PCIEX4 [page 15]

2.JACPI1 connector is from 10 pin to 14 pin. [page 32]

3.EC92 change from DIP to SMT. [page 27]

4.EC6 change from DIP to SMT. [page 27]

5.I change USB PORT from 12 to 9. [page 9]

6.I change USB PORT from 13 to 8. [page 9]

7.I change PCIE LAN port from 2 to 5. [page 9]

Placement History

1.I move JFP1 pin-header close to ATX POWER connector.

2.I move JBAT1 and BAT1 pin-header close to CPU FAN connector.

3.PCIEX1 change PCIEX4 .

7733-0D----->0E History

1.I change ddr clk 2:3 to 0:1. [page 4:7:8]


2.I change ddr ODT 2:3 to 0:1. [page 4:7:8]

3.I change ddr CS 2:3 to 0:1. [page 4:7:8]

4.I change ddr CKE 2:3 to 0:1. [page 4:7:8]

5. DDR DIMM1 SA0;SA1 (1:0--->0:0) . [page 7]

5. DDR DIMM2 SA0;SA1 (1:1--->0:1) . [page 8]

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